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JUNE 2005 VOLUME 9 NUMBER 5

Just what is a blade, anyway?

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KONTRON AT8001 CPU BOARD WITH TWO AMC MEZZANINES INSTALLED

In this Issue:

SBC Product Guide

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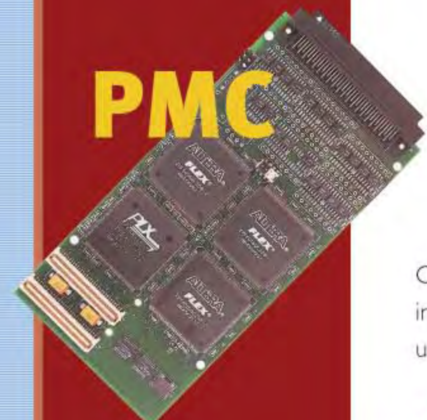
	General Standards	Leading Competitor
Power Dissipation/32 Chan	12 Watts	35 Watts
Phase Skew	55ns (0.1 deg at 5KHz)	Not specified
Crosstalk	96dB	90dB
SINAD	93dB (cPCI, PMC, & PC/104+)	86dB (cPCI), 90dB (PCI)
Gain Accuracy	± 0.1mV, ± 0.1 percent	Not Specified
Sample Rate	200K per Chan (cPCI,PCI,PMC, PC/104+)	108K per Chan (PCI) 216K per Chan (cPCI)
Industrial Temp Range	-40° to 85°C	-40° to 85°C
Commercial Temp Range	0° to 65° C	0° to 50° C
Cost (32 Channels)	$5,995 (Qty 1)*	$9,000

* Cost is for Commercial Temp Version. Quantity discounts available. Conformal coating available.



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By Joe Pavlat
Editorial Director

Uptime. Downtime.

For decades, designers and customers of embedded computer systems have attempted to establish reliability by estimating Mean Time Between Failures (MTBF). This is almost always a calculation, usually based on the failure rates of individual components as established by tables like MIL-HDBK-217. These types of methods provide an estimate of how long a system should operate before failure:

- If the components were used within their design margins
- If the components used were good
- If the circuit assemblies were properly manufactured

A lot of *ifs*. Most MTBF calculators are largely silent about things like software, which is usually the most failure prone element of any modern, complex embedded computer. And new failure mechanisms are beginning to appear. One good example is the increasing susceptibility of very small geometry integrated circuits to logic faults and failures due to radiation sources such as solar neutrons that practically cannot be shielded against (see the October, 2004 *CompactPCI and AdvancedTCA Systems* Editor's Foreword). And, MTBF is just a statistical estimate. A system with a 30,000-hour calculated MTBF may fail after a few hours of operation. MTBF's sister calculation, Mean Time To Repair (MTTR) also assumes that the right replacement part or assembly is available and is good, and that the individual performing the repair or replacement is skilled in the process. All in all, a lot of big fat ifs and guess-timates. So, are MTBF and MTTR calculations useful? Almost certainly. Are they enough? Increasingly, the answer is no.

Is there a better way?

The telecommunications industry has, for years, used availability in addition to MTBF as a better measure of a system's overall reliability and robustness. Numbers like 5-nines (99.999% uptime, or about 5 minutes of downtime a year) or 6-nines (99.9999% uptime, or about 30 seconds of downtime a year) are often used as measures of availability. Availability requires a somewhat different mindset when compared to MTBF thinking. Highly available systems are generally architected in very different ways from traditional systems. They usually have multiple, redundant resources such as processors, power supplies, and storage. Specialized hardware and software combine to detect failures and switch out bad resources and subsequently switch in good ones. Downtimes are often measured in seconds or minutes, not hours or days. Of course it is almost always desirable to replace failed resources with good ones for continued redundancy, and features like hot swap and system management help repair personnel keep the still-running system ready for the next failure. The term 24x7 is being replaced in the communications world by *3600 by forever,* which is a better measure of real world requirements. Downtimes need to be measured in minutes at most, not days.

Designers of military electronics should be interested in high availability architectures. Traditional military systems have achieved a level of reliability by robust packaging and careful component selection, but usually have simple single-resource architectures without the capability of failure tolerance and automatic repair. Additional forces are in play that should cause military electronics designers to take a few chapters from the telecommunications equipment design handbook and start to think about availability instead of just MTBF. For example, today many necessary components are of commercial grade, including almost all silicon. That's not necessarily a bad thing. One good aspect of this trend is that complex silicon gets cheaper every year, permitting the duplication of many functions for redundancy. Also, today's net-centric warfare environment is largely about information technology and communications. Many of the lessons about making those types of systems highly available have already been learned in the telecom world, including different methodologies for software robustness than those used in the military systems. Sure, environmental extremes and operating temperature requirements will often make some military electronics systems specialized, but the underlying architectures and components developed for the much larger communications marketplace should be considered wherever possible.

Keeping modern military electronics systems operating *3600 by forever* will be absolutely necessary in the future as warplanners and warfighters make rapid decisions based on real-time information. Putting the best heads together from both the telecom and military electronics worlds would be a great opportunity to further the state of the art for both and to face common challenges, such as better cooling technologies, for the future.

Joe Pavlat, Editorial Director

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Q&A: Realizing standards-based telecom systems

By Curt Schwaderer

CompactPCI & AdvancedTCA

The demand for new products and services from the telecom industry are on the increase. Telecom providers find themselves lacking the resources to develop the proprietary systems of the past, and even if they could, service providers now are demanding standards-based solutions. With these challenges in mind, I recently caught up with John Fryer, Technical Marketing Director for Motorola Embedded Communications Computing (ECC), for a Q&A on the realization of standards-based telecom systems.

John Fryer

Background

You may recall Motorola ECC by the name Motorola Computer Group. The change in name symbolizes the new perspective and approaches necessary to win business and advance the market in today's telecom environment. Historically, the Motorola Computer Group manufactured circuit boards of various form factors and made them available to the industry. The software, systems, test, and validation was done by the customer. Motorola has always promoted standards-based hardware form factors, introducing a number of CompactPCI solutions into the market. But now several announcements and products point to significant standards-based software and systems solutions that are not just development systems. For example, Figure 1 shows the software architecture of Motorola's AdvancedTCA platform architecture. All of the software from the OS to middleware and applications used to be developed internally. With platforms such as Motorola's AXP, all of the middleware is written and tested, giving network equipment providers the ability to focus on system integration and application development.

Foundation products can serve as the starting point for the deployed product solution. Motorola calls these CompactPCI and Advanced Telecom Computing Architecture (AdvancedTCA) hardware and software systems *Application-Enabling Ready Platforms.*

Q. ***Recent examples point to a real trend of the behavior of network equipment manufacturers, such as Nortel and Alcatel, changing their role in delivering cost-effective, highly reliable systems to service providers. Nortel announced they are teaming up with Motorola ECC to speed delivery of a converged multimedia services system. Alcatel announced a partnership with Motorola ECC for an infrastructure program based on AdvancedTCA. Does this signal a transition from vertical to horizontal?***

A. The industry is no longer on the fringe, but in the midst of a transition phase from vertical to horizontal, meaning that telecom equipment manufacturers are no longer developing ASICs, boards, systems, and software resulting in a proprietary system. Most equipment manufacturers are shifting their core competency to the system level by developing system-wide architecture, applications, and services so that network operators can offer more innovative voice, video, and data systems. This is a challenge for these companies' limited engineering resources.

For example, 15 years ago in the enterprise systems market you had DEC, IBM, and other vertical proprietary solutions dominating the enterprise. Today, the enterprise space is a completely horizontal market. Companies such as Dell and IBM provide cost-effective hardware platform foundations. Companies such as HP and Sun Microsystems layer on the software Operating System (OS), and middleware, then applications software companies such as Oracle and VERITAS Software layer on applications. Enterprise solutions are fast, can be easily adapted, and are very much standards-based, enabling innovation at the system and application level.

Q. ***I came across an announcement relating to IBM and a partnership to use IBM's BladeCenter products as part of the Motorola platform strategy. This struck me as potentially sending a mixed signal to the market – that perhaps Motorola was hedging its bets on AdvancedTCA.***

A. The BladeCenter strategy actually fits nicely into an end-to-end service set. The lines between telecom and enterprise are blurring. AdvancedTCA provides a robust I/O capability along with compute capability depending on the blades you put into the AdvancedTCA system. This is needed due to a lot of compute-centric things happening in the telecom back-office environment. Blade servers are used in the enterprise and are compute-centric with a dimension of I/O. As you look at the end-to-end system problem, there is a point in the middle representing a gray area. The relationship with IBM

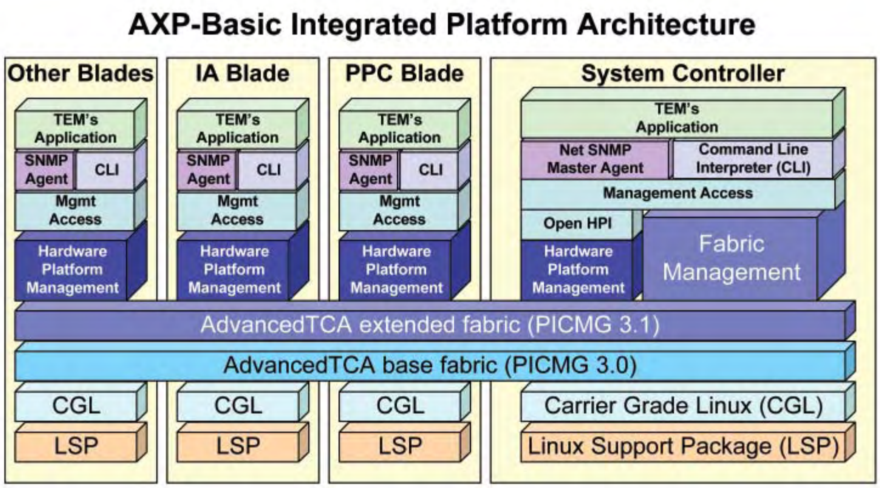

Figure 1

Where COTS was born...*and grew up!*

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and their BladeCenter products enables Motorola complete flexibility when mixing I/O and compute-centric functions within the overall system.

Q. ***All of the software from OS to middleware and applications used to be developed internally. What emphasis is Motorola putting on software services?***

A. Software is a critical component to Motorola's standards-based horizontal systems strategy. Everything moving forward is focused on standards. The basic integrated platform software – from shelf management, switch blades, controller software, and other I/O or compute blades to middleware and application software – all must be made using industry standard Application Programming Interfaces (APIs). To that end, Motorola is a significant contributor in and adopter of the Service Availability Forum (SA Forum) standards). The SA Forum Hardware Platform Interface (HPI) definitions have been approved for about a year now, and implementations appear in the Motorola systems. The SA Forum Application Interface Specifications (AIS) are newer. Only a limited set exist in their final form. We currently use a form of the AIS interfaces in our platform and plan on aggressively developing and driving these standards into products in the future.

Even beyond platforms and software, Motorola is also now providing services to do everything from thermal testing and New Equipment Building Systems/ Network Equipment Building Standards (NEBS) compliance to complete system manufacturing on behalf of their customers. These software and services enable equipment manufacturers to outsource the majority of the development of individual subsystems and focus internal resources on the task of integration, management, and applications.

Q. ***How do you gauge the industry's attitude toward a horizontal approach?***

A. We've been pleasantly surprised at the receptivity to moving toward this horizontal approach. Motorola had anticipated the acceptance of standards-based form factors, but imagined the industry would take that as a first step before going further. However, a large number of companies I talk to are making the leap from heavily proprietary to delivery of standards-based hardware and software subsystems in one step.

Q. ***One of the key differentiators between blade server companies is their robust network management and diagnostic capabilities. Might companies such as IBM see some SA Forum functionality as competitive with their network management solutions? Additionally, Motorola may find it difficult to get the information they need to properly integrate their software with software running on the BladeCenter.***

A. What we are seeing is companies such as IBM and HP becoming increasingly involved with SA Forum. Motorola anticipates future development to be complementary with SA Forum. We do not envision any Motorola software additions or integration software that would reside directly on the BladeCenter, but are not ruling it out as a future possibility either.

Q. ***Motorola has been an active SA Forum participant, most recently with regard to initial AIS specs.***

A. Motorola has taken a strong role in SA Forum and is heavily contributing. Currently, 45 companies encompassing telecom equipment, boards and systems, and software companies make up SA Forum. Telecom equipment companies Nokia and Ericsson are taking a primary role with Nortel, Lucent, and others becoming more involved.

Sun Microsystems, HP, and others are also active. Last year, B series specifications for the SA Forum AIS were introduced. This is the top end of the SA Forum charter where someone would build an application to utilize high availability services such as resource locking, message distribution, and failure event management.

The first set of AIS specifications encompasses five basic services:

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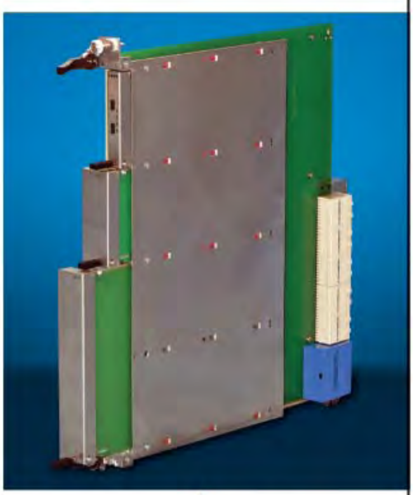

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2. Global walking: Communications and diagnostics among various node points within the system.
3. Message service: Messaging between components within a system.
4. Event distribution: Failure or management events, what constitutes an event and when it occurs, who gets notified, and how are they notified.
5. Checkpointing service: Checkpointing at certain phases within a task and if errors occur, roll back and relaunch of the task from the checkpoint.

From a telecom perspective, some of these services are enterprise-centric and too simplistic. Developers are now adding message-based distribution, system management, and logging capabilities, as well as security that figure much more importantly for telecom. Everything will now be backward-compatible from the older specifications. So, now a critical mass of services has emerged that can be adopted as a high availability system.

Q. ***What plans does Motorola have with respect to AIS?***

A. Motorola is actively developing an application interface library and plans to integrate it into our AdvancedTCA application enabling platform. Also, we plan to work with third-party platform providers to implement on their platforms as well. The HA software and AIS products will be our own unique products. In addition, Motorola plans to port the application interface library to other systems of partners that make a good strategic fit for us. The end benefit from this activity is portability for applications that perform high availability tasks within a system.

Q. ***What kind of interest are you seeing in using AIS specs?***

A. Oracle and VERITAS have joined and are seeking a way to incorporate the AIS specifications I mentioned earlier into their applications. Motorola and the SA Forum are also looking into Java-based alternatives. Since Java is quickly becoming a ubiquitous part of Internet programming, integrating AIS services, either as a Java class or native method, opens up high availability services for just about every application connecting with the Internet.

We're also seeing some activity in defense and aerospace, where the Navy and Army mandate high availability with standard form factor solutions. Many of the same attributes of streamlining supply chain coupled with high availability in telecom are also attractive for defense applications.

Significant interest also exists in the high availability SA Forum product being developed. We originally estimated one design win this year with significant design win activity in 2006, but we're well ahead of 2005 projections.

Motorola ECC is changing to meet the needs of the telecom industry. Likewise, Motorola ECC headcount seems to also be tracking this change. Currently, John estimates the ratio of hardware to software engineers being 60/40. Software head count could reach the point where the 60/40 ratio could flip in favor of software engineering over the next few years. Boards and platforms are still an important piece of the Motorola solution. However, software capabilities are the key ingredient to serving the needs of capturing new business in the telecom industry.

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Strong business

By Hermann Strass

European business trends

Alcatel, (France), one of the top five carriers operating globally, has announced their endorsement of AdvancedTCA at the 3GSM World Congress held in February, 2005 in Cannes, France, as its preferred architecture for the evolution of its mobile and fixed network infrastructure platforms. This comes after a year of working to define and develop modular communications platforms built upon AdvancedTCA, Carrier Grade Linux, and other standards. Alcatel claims this to constitute one of the world's first applications of AdvancedTCA network equipment. There are other claims such as this (see the July/August 2004 *CompactPCI and AdvancedTCA Systems,* Technology Update column). Established on May 31, 1898, Alcatel, with sales of 12.5 billion EURO (approximately $16.25 billion) in 2003 (42 percent in Western Europe) operates in more than 130 countries.

The Alcatel Evolution 9130 Base Station Controller (BSC), based on AdvancedTCA architecture, is one of the elements of a radio network. It offers up to 2,000 channels in one rack. These BSCs are the physical link between the switching center and base stations. They provide control of handovers, frequency use, and signal power control for every mobile user.

Kontron, (Germany), sees itself as the number three supplier of open-standard embedded systems products worldwide behind Motorola and Advantech. About 50 percent of their business is in Europe and 40 percent in the US. Their Compound Annual Growth Rate (CAGR) last year in EURO currency was about 20 percent (30 percent in US dollars). With almost 70 percent in capital resources, their business has a solid foundation. It is interesting that a major part of their business is in computing and control equipment for slot machines in Las Vegas gaming establishments. Kontron sells modules, systems, and applications to OEMs rather than to end users.

As with many European companies, Kontron sells into the transportation markets. Railways (rolling stock and control equipment) in Portugal, Spain, and Corsica are equipped with a variety of Kontron supplied control equipment. OEM customers in transportation include Bombardier and Siemens. A typical train management system may use devices from several product families such as:

- An information panel (12-inch TFT controlled by an E2Brain)
- Communications networks
  - Wire Train Bus (WTB)
  - Industrial Ethernet
  - CAN
  - PROFIbus
- CompactPCI systems
- Remote I/Os

Advanced Mezzanine Cards

Despite the recent collapse of the telecom market, Kontron envisions a 10 percent CAGR in this market fairly soon. Three types of AdvancedTCA boards: CPU, Hub, and Advanced Mezzanine Card (AMC) are currently available to the public and some others to undisclosed OEMs. Kontron sees a great future in AMCs as mezzanines on AdvancedTCA boards and perhaps an even better future in the form of MicroTCA. One example is AMCs that plug into a backplane directly rather than as mezzanines on an AdvancedTCA carrier board. Figure 1 shows the Kontron AT8001 CPU board with two AMC mezzanines installed. The Xeon Nocona based CPU features PCI Express, Fibre Channel, and Carrier Grade Linux. It is too early to speculate on this new application since

Figure 1

AMCs are not yet widely available. Their specification was ratified January 3, 2005 by the PCI Industrial Computer Manufacturers Group (PICMG). AMCs use card-edge connectors suitable for telecom office application versus gas-tight pin-and-socket connectors, which are required in many industrial applications as a protection against aggressive gases, moisture, and other factors.

European market analysis

Every year in time for the CeBIT Fair, the European Information Technology Observatory (EITO) issues their statistics and market analysis report derived from European and US sources. The EITO is a European organization supported by private and semi-government organizations throughout Europe. Their statistics indicate an Information & Communication Technology (ICT) market of about 1,959 million EURO (approximately $2,547 million), with Europe ahead (32.2 percent) of the US (29.4 percent) and Japan (14.8 percent). The European market breakdown of 594 million EURO (approximately 722 million) shows datacom and networking equipment at 37 million EURO (6.3 percent). Only the computer section is larger at about double this size at 12.4 percent. Overall growth rate in the EU was +3 percent in 2004 (+2.9 percent in the US), and should be +3.8 percent in 2005 in the EU. Regulatory requirements such as WEEE (see the April 2005 Technology in Europe column) or Registration Evaluation Authorization of Chemicals (REACH), and others account for some of the additional growth rate.

SBS Technologies (Germany) continues to grow in Europe (see the October 2004 issue of *VMEbus Systems* magazine, VMEbus Technology in Europe column). During the first nine months of fiscal year 2005 (ending March 31, 2005) SBS reported a sales increase of 60 percent (10 percent of which was due to the currency exchange rate) for the European Group and a five percent increase for the Americas Group. SBS is expanding their production and office space in Augsburg,

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Germany on company property. See Figure 2. The Lord Mayor of Augsburg participated in their topping-out ceremony at the end of April to honor this forward-moving company. Augsburg is an old but very innovative city. Together with Trier, it shares the title of being the oldest city in Central Europe that is in today's Germany (countries such as France and Germany did not exist in those days) with more than 2,000 years of recorded history. The physics department of the University of Augsburg is world class with some significant breakthrough discoveries announced this year. The Augsburg region is perhaps the world's foremost center of excellence in environmental research and development (see the April 2005 issue Technology in Europe column). Mozart's parents and their ancestors come from Augsburg. Rudolf Diesel invented the diesel engine at Augsburg. So SBS European headquarters (within a stone's throw from Augsburg University) is *embedded* in an innovative, *environmental*, and historical environment. SBS develops advanced products using AdvancedTCA and MicroTCA technology. SBS has developed an AMC processor board, to be announced in time for the International Supercomm Conference in Chicago, June 6 to 9, 2005.

Figure 2

Hermann Strass *is an analyst and consultant for new technologies, including industrial automation, computer bus architectures, mass storage technologies, and industrial networking. He is an active member of several national and international standardization committees.*

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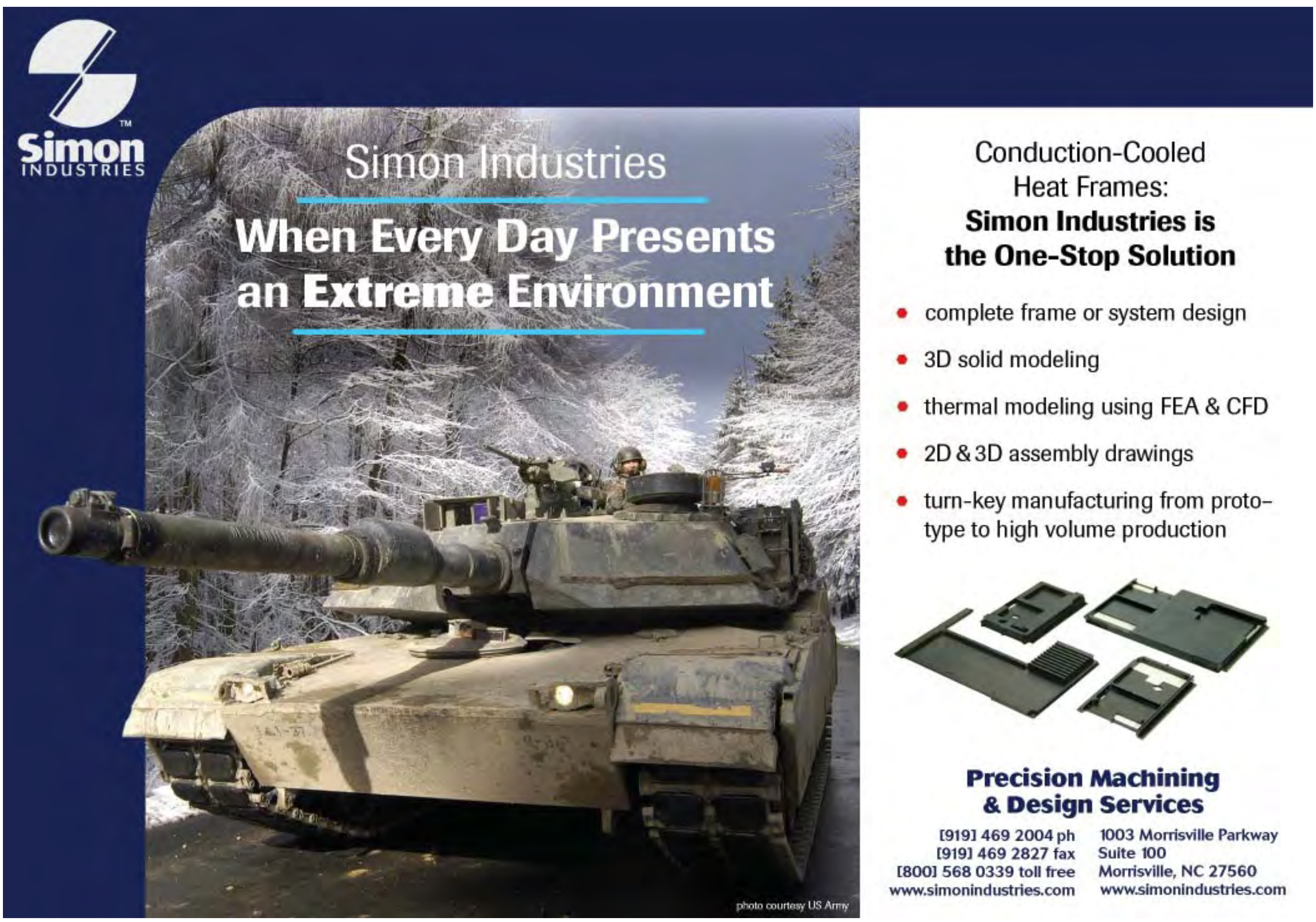

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MILITARY APPLICATION

CompactPCI in the military: Playing to its strengths

By David Compston

David discusses the advantages CompactPCI's inherently I/O-oriented architecture yields for network-centric warfare and the need for smaller, lighter solutions.

To understand where CompactPCI fits in the military scheme of things, and the factors that will affect its future, it's important to understand "the nature of the beast." How is the military different from, for example, the telecommunications marketplace – and how does this difference affect its adoption of new technologies?

The first thing to understand is that the overriding characteristic of the military marketplace is its inherent conservatism. Making technology decisions that can literally be a matter of life or death – rather than a bad telephone line connection – makes you somewhat cautious. The ideal military technology is stable, proven, known to be reliable, and widely accepted, attributes more highly prized than cutting edge performance.

It is also true that, given the typical military application's complexity, its manner of deployment, and the nature of how that development and deployment are funded, vendors measure project timescales in years or very often in decades. This forces attention onto issues such as obsolescence mitigation and long term support, again causing the military to value technologies that have proven longevity. Beyond this, the military faces the requirement to integrate with an enormous installed base of legacy systems. As a result, development tends to be evolutionary, rather than revolutionary.

This approach often meant that, historically, the military struggled to stay abreast of technology developments. The landscape changed, however, with Senator William Perry's memorandum of June 1994 which, in effect, mandated that in the future the US defense industry, which represents a huge proportion of the defense industry worldwide, should no longer design and develop its own proprietary solutions, but should rather take advantage of the substantial cost savings available from implementing Commercial Off-the-Shelf (COTS) solutions instead. Although primarily intended as a cost-saving measure, COTS brought new technologies to military applications more quickly and, through adherence to industry standards, delivered the high degree of interoperability that was fundamental to the military's requirements. The COTS approach has also reduced the time to market for new applications.

The foregoing may give some insight as to why it is that CompactPCI has not thus far made the progress in the military market that might reasonably have been expected, especially given the pervasive nature of PCI technology both on the desktop, and as enabling technology for the majority of boards sold into military applications. Although PCI has been around for 10 years, it is still, in military eyes, a newcomer by comparison with VMEbus. VMEbus is the bus architecture at the heart of the majority of military systems and has been around for a quarter of a century. The history of VMEbus is a remarkable one, not least in the ability it has consistently demonstrated to embrace and adapt to emerging technologies.

But if the advent of COTS opened the door to CompactPCI, it is the real change in military thinking that is likely to see it establishing at least a substantial toehold. The buzz phrase in military circles is *network-centric warfare,* and it describes a new paradigm in which military "appliances" are viewed as nodes on a network, with local electronic intelligence at the point of deployment. Future battles will be won by the force that can most quickly gather, analyze, distribute, and act on information. That's nothing new in warfare, of course.

An important goal of network-centric warfare is that it should be technology-intensive, not personnel-intensive. "Sensor to shooter" solutions, for example, capture the idea that a potential target can be identified, acquired, and dealt with in a single, seamless electronic process that requires no human intervention. Unmanned vehicles, whether Unmanned Ground Vehicles (UGVs) or Unmanned Aerial Vehicles (UAVs), are the next logical step in this direction.

Limits to VME 3U implementations

While either can be of any size (a UAV, for example, can range from a hand-launched unit to one which requires a traditional runway) the trend is towards small and lightweight to maximize both deployability and mission range. This trend presents something of a conundrum to designers of military systems, because it points to the need for a solution built around the 3U form factor. VMEbus, which would otherwise be the natural choice, does not readily lend itself to "small and lightweight." Designed for high performance, multiprocessor applications in harsh environments, VME is highly scalable, but its 3U implementation has three important limitations. The first of these is that VMEbus systems are power-hungry, and thus generate heat that has to be dissipated. Second, the full 64-bit implementation of VMEbus is only available in its 6U format. This creates performance constraints for the smaller systems, which may only use the 16-bit implementation. Third, and perhaps most importantly, VMEbus in its 3U form provides negligible rear I/O, greatly reducing its flexibility.

CompactPCI, on the other hand, provides an architecture that is inherently I/O-oriented, with the availability of 75 pins across the backplane. Its 32-bit parallel bus offers potentially higher performance than VMEbus in its 3U form. It is designed to support a maximum of 8 slots – compared with VMEbus's 21 slots

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– and consumes less power. Typically, as the components are closer to the cooling rails, conduction cooling can be more efficient.

Building a UAV around a 3U CompactPCI solution, such as Radstone's RT4 PowerPact application-ready platform, can generate substantial savings in weight, size, and power consumption. Figure 1 shows the RT4. The RT4 measures approximately 10 inches by 5 inches by 5 inches, making it less than a sixth of a cubic foot in volume, and it weighs less than eight pounds. Yet it delivers the same processing power as Radstone's PPC7D processor in a 1/2 ATR chassis, which weighs more than twice as much and occupies 25 percent more space.

Lightweight design surveillance radar

Perhaps typical of the military applications for which CompactPCI is well suited is the development being undertaken by Telephonics Corporation, headquartered in Huntington, NY, for Lockheed Martin in support of the US Coast Guard's Deepwater program. Targeted at the emerging market that is demanding fully capable surveillance radar in a lightweight (less than 75 lbs.), compact (two boxes – 1/2 ATR Short Signal Processor and 3/4 ATR Short Receiver/Transmitter) design, and developed for use in UAVs, the project selected CompactPCI because of its combination of higher bandwidth (relative to VMEbus), support of a lightweight 3U form factor, and interconnect ability (via the PCI backplane). Beyond this, the inherently open architecture of CompactPCI gives Telephonics access to a range of products from potential suppliers, together with a powerful road map via PCI-X and PCI Express. The company believes that the industry trend towards Maximum Radar Processing capabilities, Digital Scan Conversion, and interfaces to programmable gate arrays in the area of signal processing, together with the increasing emphasis on remotely oper-

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Figure 1

ated (unmanned) platforms and smaller, lighter solutions will see CompactPCI continuing to gain acceptance in the defense community.

CompactPCI in its 3U form offers benefits for space-, weight-, and power-constrained applications that are very attractive to the military system designer. Beyond this, the growing number of conduction-cooled CompactPCI boards is increasing all the time, and the nature of the technology means that it is possible to develop extremely powerful but relatively inexpensive solutions: Radstone's IMP2A (see Figure 2) CompactPCI processor, for example, has the functionality of a 6U card in a 3U space.

Although it is "immature" by VMEbus standards, the military market is reassured by the comparative longevity of CompactPCI, noting that it has not only survived but also thrived in an industry that seems to throw up new bus technologies every month.

But just as CompactPCI seems to be coming into its own in the military marketplace, questions are arising about its future. The desktop PCI architecture on which CompactPCI is based is moving rapidly towards PCI Express with its substantially improved performance. PICMG has intercepted the concern with its proposals for 3U Express (and 6U Express), which will provide a native PCI Express backplane in the CompactPCI format and accommodate legacy CompactPCI cards.

While the military may be wary of the transition to a new backplane, VMEbus is going through a similar transition with the VITA 46 proposal that is designed to accommodate upcoming switched fabric

Figure 2

technologies with a redesigned backplane. In the case of VITA 46, military customers have indicated a willingness to accept change if it delivers higher performance – and it seems likely that hybrid solutions will emerge in the case of both VITA 46 and CompactPCI.

When CompactPCI was first announced, some commentators believed that it was conceived as a competitor to VMEbus. That proposition has always seemed unlikely, given that the two technologies have contrasting strengths and weaknesses – which is why, today, it looks as if they will coexist in the military market space, with CompactPCI leveraging its strengths to take advantage of the move towards smaller, lighter solutions. Manufacturers such as Radstone will continue to offer products based on both architectures.

***David Compston** graduated from the University of Warwick, England with a degree in Computer Science. He is a board industry veteran, having held lead positions both in engineering and marketing for Radstone for more than 20 years. David is currently Director of Marketing for Radstone Embedded Computing.*

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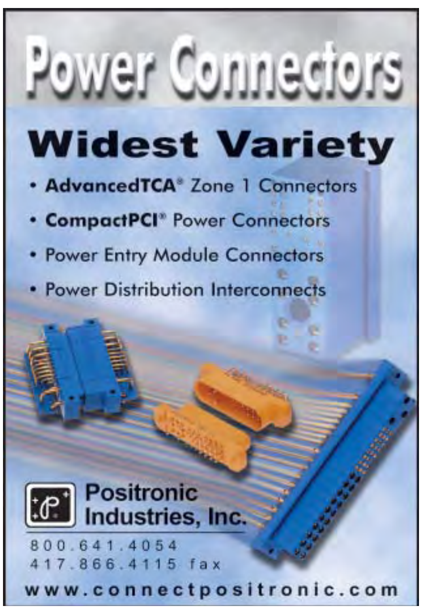

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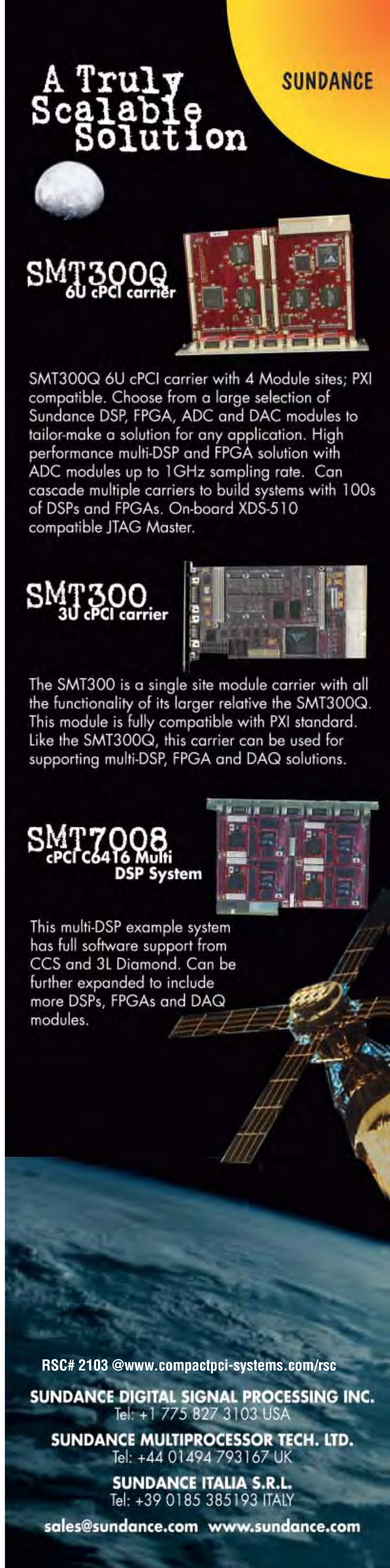
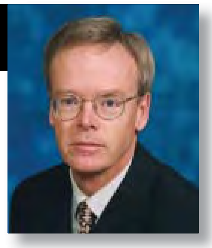


Beam-forming to scientific modeling: High-density compute platforms offer multiprocessor solutions



By Ian Stalker

The CompactPCI standard continues to grow in importance for high-end applications. There is for example increased demand for Gigabit Ethernet in a PICMG 2.16 configuration. This marks a step towards the eventual replacement of parallel bus technology with switch fabric interfaces, yet it must be stressed that the new generation of switch fabric technology such as used in AdvancedTCA is still some time away from maturity and general deployment. In this article Ian covers a number of applications that make use of this type of technology, signal analysis being one of them.

Today, the preponderance of CompactPCI applications are served by classic general purpose Single Board Computers (SBCs) and I/O products, where a single microprocessor, paired with application specific I/O, provides sufficient computing power to perform the requisite task. Many industrial control applications, for example, fall into this category. At the other end of the performance spectrum reside applications that are essentially *compute bound* meaning that the system designers will take advantage of as many MIPs and GFLOPs as their fiscal or power budget will permit. Simulation and scientific modeling are examples where there is continual need for greater speed and resolution, and which also frequently require multiprocessor solutions.

Two classes of compute problems need multiprocessing solutions. The first class comprises *compute farm* applications where multiple channels of data need to be processed but have only a small or medium requirement for interchange between the processors working on the problem. For these applications Ethernet provides an ideal transport between the processors because it is simple to program with portable software and is also cost-effective. Scaling up to large systems involves the relatively straightforward process of packaging multiple boards into enclosures.

The second class of multiprocessor applications is that in which multiple processors work with a shared database on a single problem. These problems typically involve large amounts of interprocessor communications. One example of this type of application is digital radio beamforming. In these applications one would benefit from augmenting the interboard I/O with a higher performance, low overhead communications technology.

A high-density 6U CompactPCI compute platform based on the PICMG 2.16 Packet Switching Backplane (cPSB) standard, such as Curtiss-Wright's CHAMP AV-IV (CAV4) can be adapted to these applications with the addition of one or two StarFabric PMC modules to provide up to approximately 1 GBps of interboard I/O while significantly reducing processor overhead. Figure 1 shows the CAV4.

Figure 1

PICMG 2.16 plus

As previously mentioned, the CAV4 employs the PICMG 2.16 Packet Switching Backplane standard. In fact, the CAV4 does not have a PCIbus backplane interface. The PICMG 2.16 standard was developed to overcome the inherent limitation of the PCIbus. With a single, shared, parallel bus capable of 533 MBps (best case, 5-slots), CompactPCI systems were becoming limited by the throughput of their interconnect. The PICMG 2.16 standard introduced the concept of using Ethernet (10/100 or 10/100/1000) as the main data transport mechanism within a system. Using the CompactPCI midplane J3 connector, the standard defines node and fabric slots. Node slots have one or two Ethernet interfaces. Fabric slots provide the Ethernet switching function. Systems comprise one or two switch cards, and up to 20 nodes, supporting a total bandwidth of up to 5 GBps.

The CAV4 extends the PICMG 2.16 principle even further. It provides five Gigabit Ethernet interfaces to the backplane connectors. Each processing node, including the 8540 control processor, has an independent Ethernet connection to the backplane. Two of these interfaces are on the pins defined by PICMG 2.16.

Systems built using the PICMG 2.16 Ethernet standard are precursors of the new era of interprocessor communications using switched fabric technology. Standards such as VITA 41, VITA 46, AdvancedTCA, and CompactPCI Express are all based on high-speed point-to-point serial interconnect with switching instead of buses. While these technologies continue to mature, Ethernet will garner many design wins for the current generation of systems.

Ethernet performance

In the course of characterizing the performance of the CAV4, the Ethernet throughput was measured using the Wind River Systems VxWorks real time operating system with the *Blaster/Blastee* test programs that are included. These programs have two tunable parameters: transmit message size and receiver buffer size. The best performance, not surprisingly, was obtained with the largest message sizes. The test used the standard VxWorks 5.5 IPV4 network stack without optimizations to take advantage of the Discovery III TCP checksum offload feature. Table 1 shows the performance obtained using PowerPC

7447A processors at different clock rates using message sizes of 48 KB.

With a total of five Gigabit Ethernet interfaces, the card is capable of well in excess of 300 MBps throughput. A system comprised of many CAV4s would have dramatically more Ethernet communications bandwidth than that provided by a single PCIbus.

Power consumption

It is a well-known phenomenon that the power consumption of microprocessors and accompanying system logic has been steadily rising. Desktop processors from Intel and AMD now top 100 W. In high-performance multiprocessor computing applications, the *name of the game* however is computing density. The question is, "How much real computing work can be accomplished within the confines of standard enclosures and racking systems, without resorting to prohibitively expensive cooling technologies such as spray cooling or refrigerated air systems?"

The latest generation of quad processor designs is starting to push the envelope of available cooling in the IEEE 1101.10 mechanical standard. A precision air mass-flow measurement test was developed by Curtiss-Wright to qualify and accurately specify the cooling requirements for high-power, air-cooled processor boards. In concert with this program, we have characterized the power consumption of the Compact CHAMP-AV IV at different processor clock rates and inlet air-temperatures. Table 2 shows the power for a test scenario designed to stress the processors and memory subsystem of the card, thereby consuming power in excess of the majority of real applications.

These tests highlight some of the factors that influence power consumption. Faster clock rates are usually accompanied with the need to power the processor core at higher voltage, causing relatively large increases in power for relatively modest increases in clock rates between 998 MHz and 1064 MHz. The other factor that is perhaps less well understood is processors' drawing more power when running at higher silicon die temperatures, illustrating the need for effective thermal designs and air-management within the enclosure. Freescale's power estimates for the 7448 processor are not publicly disclosed, but we expect to see power reductions at equivalent test conditions.

Much of the technology required for applications with high performance needs in the military market such as radar, sonar, and signal intelligence can be applied in products aimed at the high-end of the commercial/industrial CompactPCI market space where performance and packaging density is valued but extreme ruggedization is not.

Ian Stalker *is the DSP product manager for Curtiss-Wright Controls Embedded Computing. He holds more than 20 years of experience in the embedded industry and has a degree in Electronic Engineering.*

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Processor Clock	Ethernet Performance
665 MHz	62.6 MBps
998 MHz	79.1 MBps
1064 MHz	79.1 MBps

Table 1

Core Voltage	1.0 V	1.0 V	1.1 V
Core Frequency	665 MHz	998 MHz	1064 MHz
Average Power @ 25 °C inlet	47.6 W	54.7 W	64.9 W
Average Power @ 50 °C inlet	50.6 W*	59.2 W	70.9 W

*Power measured at 40 °C for this test.

Table 2

Processing challenges of shrinking high-end embedded computing systems to fit into small unmanned air vehicles

By Bob Kahane

Large Unmanned Aerial Vehicles (UAVs) such as Global Hawk and Predator have been successful using today's high performance embedded computing solutions. In this article Bob explains that the challenge is to provide similar processing power for much smaller UAVs, many of which have less than half the payload weight and one-quarter the volume of the Predator.

UAVs offer an ability to perform penetrating surveillance missions as well as *persistent surveillance* with low risk and the ability to *get in close* to better see, hear, and sense the situation of interest. One of the best-known UAVs is the Global Hawk, a multimillion-dollar aircraft managed as a theatre/national asset similar in dimensions to the U2 manned reconnaissance platform. The Global Hawk, with its large size, provides a platform for multispectral sensor suites, including Synthetic Aperture Radar (SAR), Electro-Optic/Infrared (EO/IR), and SIGnals INTelligence (SIGINT) payloads. This UAV has proven its worth in battlefields from Bosnia to Afghanistan and Iraq. This success has led to a surge in proposed UAV missions and designs using a layered approach, with multiple classes of UAVs to provide persistent narrow and wide Intelligence, Surveillance, Reconnaissance (ISR) coverage. In support of this mix, smaller UAVs, such as the Hunter and the Predator, are most widely known and have also proven their utility with a lesser complement of sensors. When netted with manned and larger UAVs, smaller UAVs provide significant synergy and effectiveness in rapidly assessing the situation. In addition, smaller UAVs can detect targets of interest with high accuracy and with targeting quality geolocation.

Large UAVs such as the Global Hawk and Predator-B have been successful using today's high-performance embedded computing solutions. The challenge is to provide similar processing power for the newest UAVs, which are significantly smaller, and many of which have less than half the payload weight and one quarter the volume of the Global Hawk (Table 1).

UAV	Global Hawk	Predator B	Heron A	Hunter	Eagle Eye	Fire-Scout	Sentry	Dragon Warrior	Dragon Eye
Picture									
Length (ft)	44.4	36	26	22	17	23	8.4	10	3
Wingspan (ft)	116	66	54	29	17	20	12.8	9	3.8
Height (ft)	14	9.5	5.9	5.6	5.5	9.5	4	5	1
Payload Weight (lbs)	1000	800	550	250	200	200	75	35	5
Max Altitude (ft)	65k	50k	25k	15k	20k	20k	15k	4k	1.2k
Sensors	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR SAR ISAR SIGINT MTS	EO/IR	EO/IR	EO/IR
Endurance (hrs)	36	36	36	10	5	4	3	3	1
Max Airspeed (kts)	320	220	120	100	220	120	100	70	35

Table 1

System demands

UAV platforms must have signal processing systems that can function under difficult environmental conditions, covering high humidity, extreme heat and cold, dirty air, high altitude, shock, and vibration. Usually UAV platforms must deal with some or all of these challenges at the same time.

Despite restrictions on payload size and weight, the new signal processing systems must be highly flexible. The cutting edge of defense imaging technology combines multiple types of sensors in a single platform, giving field commanders a full-spectrum view of the battlefield. Rapid access to multiple types of images for their specific situation enables these commanders to make more informed, more effective combat decisions. The addition of SIGINT payloads for electronic-support type missions, such as Radio Frequency (RF) emissions, are characterized as to emitter type, class, and angle of arrival, and increase the effectiveness of the imaging sensor. SIGINT payloads provide passive, 360-degree surveillance across wide RF bands of interest and can cue narrow field-of-view imaging sensors to rapidly detect activities of interest.

The most powerful example of this multisensor approach is the Integrated Sensor Suite (ISS) deployed on the Global Hawk. Raytheon developed this powerful imaging system, with signal processing supplied by multicomputers from Mercury Computer Systems. SAR imagery enables operators to view wide areas of terrain, while high-Doppler resolution radar provides a Moving Target Indication (MTI) capability that can identify individual moving vehicles, or even the recoil motion of artillery tubes.

Multisensor imaging capability has proven to be highly effective. Operation Iraqi Freedom employed a single Global Hawk; it flew just 3 percent of all imagery-collection sorties, yet it generated 55 percent of all the time-sensitive targets passed to attacking units.

These results are driving plans to put multisensor systems on more of the newer, smaller UAV platforms, as well as to expand multisensor capability into hyperspectral imagery and ultrawideband (UWB) radar for penetrating foliage. To support the multisensor approach, signal processing systems must be able to generate imagery from a shifting and variable set of sensor inputs. They must be able to perform a set of diverse functions and interface to a broad range of sensors.

In the past, we have relied on Moore's Law to help us out. We could wait a couple of years and the technology improvements in the electronics would have enabled significant size and power reduction. However, the industry has reached a point where Moore's Law still increases absolute performance, but not performance per Watt, per pound, or per cubic foot. Although the number of transistors available is increasing, the power consumption is increasing at almost the same rate (see Figure 1). The increased infrastructure to handle the power distribution and heat extraction incurs a penalty in size and weight. Alternative approaches are needed.

System expectations

As the platforms get smaller, the sensor systems are driven to greater challenges in meeting the performance requirements within smaller envelopes of Size, Weight, and Power (SWaP). In addition, reduced

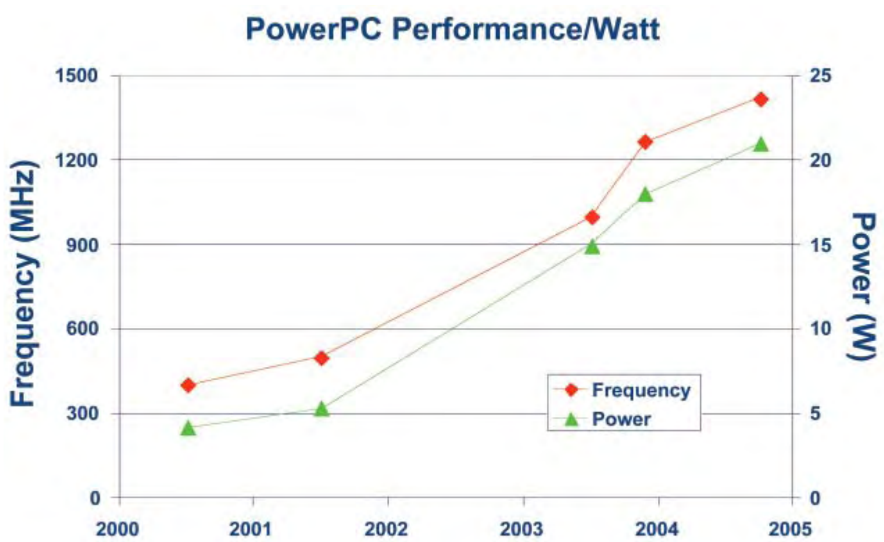

Figure 1


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platform size is driving developers to dramatically reduce the cost of the payloads. What's needed are attributable platform-payload solutions that still exhibit appropriate levels of reliability to match the forecasted life expectancies of the platform. A first-order approximation of system flyaway costs is $10,000 per pound. This figure was developed many years ago on a multispectral Electronic Warfare (EW) system development involving six major EW companies and has survived many technology shifts. Technology has provided more capabilities per pound, but this approximation has still proven to be adequate for rapidly approximating system costs.

System requirements

The first basic requirement is that the signal processing systems must be physically small enough to fit into the new platforms. For many platforms, the commonly used 6U VME systems are just too big; 1U, 2U, or 3U form factor solutions are needed. In addition, the signal processing systems must adhere to industry standards for board design and interfaces, if systems designers are to benefit from Commercial Off-the-Shelf (COTS) solutions.

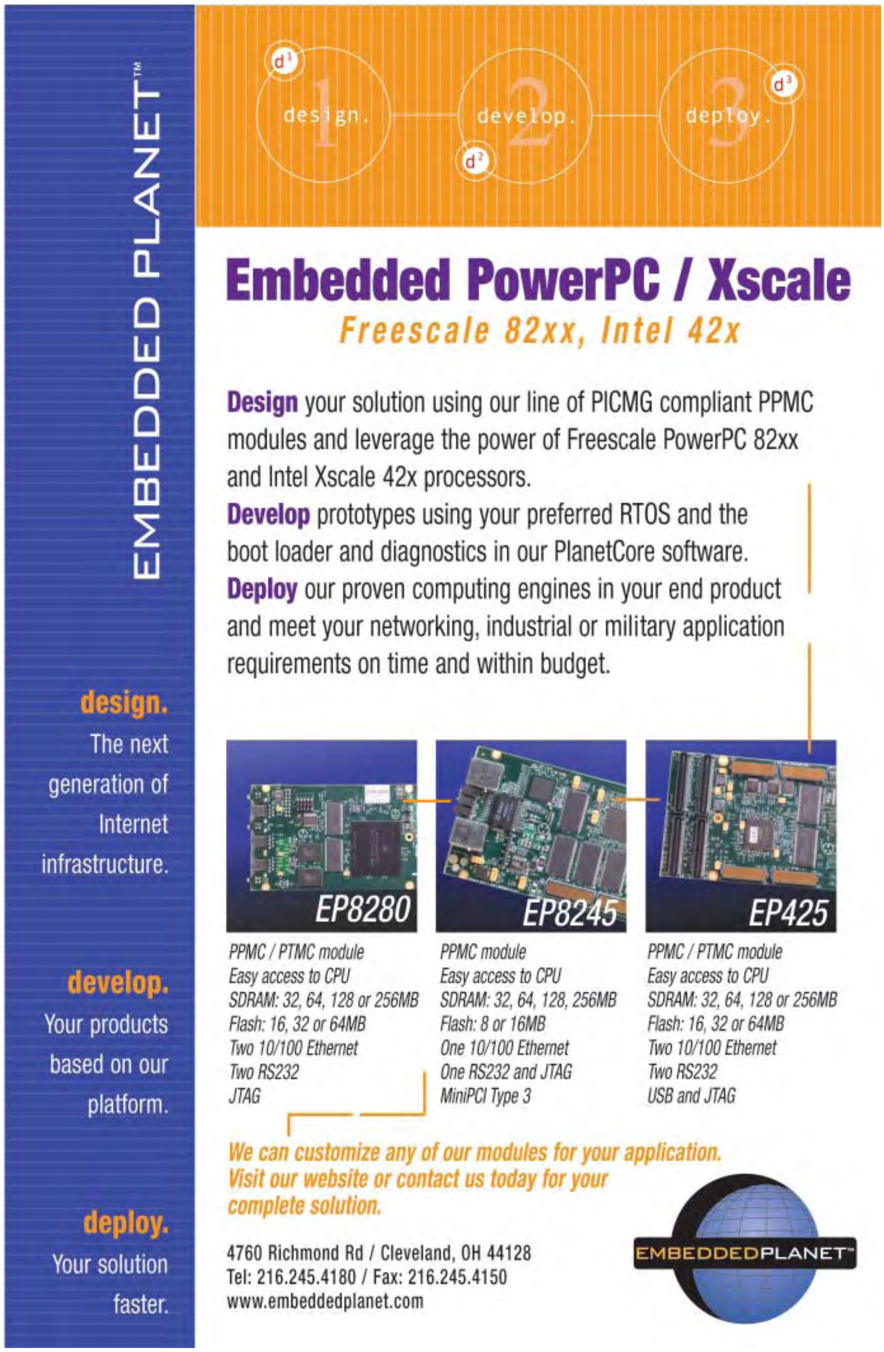
Squeezing the processing power of 6U boards into smaller form factors demands the creative use of a specialized adjunct processor. Adjunct processors are devices such as Field Programmable Gate Arrays (FPGAs) and ASICs, dedicated to a specific computationally intensive operation. Because adjunct processors execute a single task, they can do it with extraordinary speed and efficiency. Developers can partition signal processing operations among different types of processors for maximum efficiency, getting more done in less space while accepting the tradeoff of somewhat greater system complexity. True multisensor flexibility demands the signal processing engine have a variety of I/O options, all with high-bandwidth interconnects to the processors. Ideally, these I/O options connect directly to the processing boards, as well as supporting some form of an industry-standard mezzanine card.

Since engineers develop functional software according to an overall project schedule, they need access to adequate development tools, including algorithm libraries and I/O device drivers. If adjunct processors are employed, efficient development tools must support them. And lastly, because these systems are often called upon to operate in harsh environments, they must be able to withstand shock, vibration, and temperature extremes.

Processing density and efficiency

One approach for achieving processing density and efficiency for signal processing is to leverage adjunct processing engines such as FPGAs as programmable processors. For some front-end signal and image processing functions, FPGAs have demonstrated a 10- to 20-fold performance boost over a PowerPC G4 processor. However, some front-end tasks, such as filter weight computation and most back-end processing, still perform much better on a PowerPC processor. In fitting the most processing power in the smallest space for a given application, the trick is finding not only the optimum balance between FPGAs and PowerPCs, but also determining exactly which model of each chip to choose.

Application software can be partitioned so that certain algorithms go onto the FPGA. FPGA-appropriate algorithms include fixed-point computations or non-



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data-dependent operations. Other parts of the application, especially data-dependent operations, are targeted to the general purpose processor, which is easier to program for those types of algorithms. This style of application partitioning maximizes system performance while keeping overall development time manageable.

Solution design

Several approaches provide more capability in smaller physical configurations. The first is the use of dense packaging in physically small but standard configurations. Another approach is the sharing of processing across multiple sensors. This technique provides multimission processing from a common set of processors. The technique supports multiple payloads and provides time-sliced load-leveled solutions across a suite of sensors that operate virtually simultaneously, providing short yet effective periods where processing elements can be shared.

For physically small but standards based design requirements, 3U CompactPCI is a strong choice. It is a widely accepted standard, maximizing configuration flexibility with a wide range of market-available products. The 3U CompactPCI connector offers outstanding pin density; the J1 and J2 connectors provide enough pins to support 32-bit PCI with additional pins left over for sensor I/O. Because it uses PCI as the system bus, CompactPCI also delivers compatibility with system software components. Standards-based I/O flexibility can be further supported with a PCI Mezzanine Card (PMC) interface; PMCs are a common enhancement to 3U CompactPCI systems.

Development of multimission computing payloads provides significant opportunities to the platform primes as well as to payload developers in realizing increased individual sensor processing resources within the SWaP and cost constraints of the platform.

Example system

Mercury Computer Systems' MCP3 FCN module meets these requirements, delivering highly flexible signal processing capability in a space-efficient 3U CompactPCI format. (See Figure 2.) The MCP3 FCN employs a 1 GHz PowerPC 7447 and a Virtex II Pro P40 FPGA. A Discovery II bridge chip connects the two processing units. The three avenues for off-board communications and I/O are via:

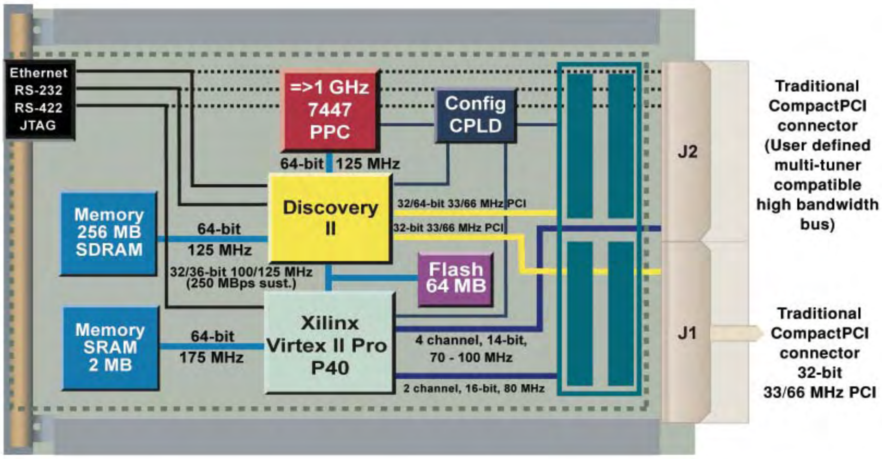

Figure 2

- PCI bus on the J1 pins of the CompactPCI connector
- Digital Intermediate Frequency (IF) to the FPGA via a direct connection from a subset of the user-defined J2 pins
- PMC, which can communicate directly with the FPGA or through the Discovery II chip to the PowerPC

To develop application components targeted for the PowerPC processor running Wind River's VxWorks operating system and using the Tornado operating environment, engineers have access to a mature set of Mercury tools, including the Scientific Algorithm Library (SAL) with more than 600 routines optimized for the PowerPC. For those parts of the application that run on the FPGA, developers can use Mercury's FPGA Compute Node Developer's Kit, or FDK. This kit is a collection of Mercury-developed Intellectual Property (IP), build files, command line tools, libraries, headers, drivers, board descriptors, diagnostics, and consulting support, all focused on helping engineers efficiently create reliable FPGA-based applications.

The MCP3 FCN board is also capable of deployment in harsh environments. It is available in both air-cooled and conduction-cooled versions and is optionally delivered in either an IEEE 1101.1 or DRTi chassis. This type of space-efficient 3U signal processing solution can be built using powerful COTS components, including Mercury's MCP3 FCN. It is small enough to be used in smaller platforms such as UAVs, and flexible enough to perform multiple missions and interface to a variety of sensors.

Conclusion

The processing requirements of smaller UAVs can be met today with the careful allocation of the requirements to the available COTS processing/adjunct elements in smaller, denser yet standard packaging configurations. These systems can meet the environmental challenges and performance requirements of affordable flyaway costs, appropriate reliability, and performance to support the multisensor requirements within the platform's SWaP constraints.

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Carrier Grade Linux: The cornerstone of telecoms' COTS strategy

By Glenn Seiler

The telecommunications industry is in a state of profound change and is now beginning its long rebound from the burst of 2001. The industry is finally starting to see significant consumer demand for 24x7 accessibility to multimedia-based high bandwidth services. Of course consumers want these new services for less than they used to pay for standard voice service. This demand is driving the rapid growth of Next Generation Networks (NGNs) and thus provides opportunity for increased revenues and market share, if the service providers can react to the market. But this increased opportunity is also causing the emergence of new competitors to service these markets. These new competitors do not have the large inventories and cost structures that were created prior to the burst. Service providers are faced with the challenge of providing new services while continuing to reduce capital and operation expenses. These service providers must find cost-effective methods to drive down costs and get higher margins in return for their services.

Convergence and transformation

This change is having a far-reaching impact on the entire supply chain of ISVs and operating system suppliers, semiconductor and hardware component vendors, and most importantly the Network Equipment Providers (NEPs). NEPs can no longer afford to develop entire solutions in-house and must focus their resources on the development of new value-added services. A key strategy to drive down and manage costs is to develop systems for new markets using common Commercial Off-the-Shelf (COTS) components for software and hardware. These COTS components are transforming the telecommunications industry just as they did for the enterprise and IT industries in the 1990s when volume-based x86 servers running UNIX and later Linux began replacing single-vendor proprietary hardware and OS solutions.

In fact, the convergence of application services and network infrastructure applications is one of the key forces driving telecom COTS ecosystem growth. For a long time the telecom industry has been using proprietary hardware solutions with proprietary real-time carrier grade operating systems, often built in house, and in-house high availability and management solutions for their network infrastructures. At the same time they often use commercially available IT or enterprise-based solutions for application services such as BSS and OSS. But now commercially available Carrier Grade Linux-based systems offer the real-time support and high reliability the network infrastructure requires. These Carrier Grade Linux systems combined with advances in commodity processor and hardware technology are driving COTS into the previous proprietary network infrastructure. By leveraging the benefits of these COTS components many NEPs are now developing a *universal platform* comprised of COTS components that support both application services and traditional network infrastructure services in a single cost-effective platform. NEPs can now use commercially available common components to replace much of the in-house R&D development for both hardware and software, creating significant savings. This drives the creation of standardized hardware solutions such as AdvancedTCA packaged with carrier grade operating systems and third party high availability solutions. This trend is shown in Figure 1.

In particular, it is the NEPs and their customers, the service providers, who are driving this trend. They have the most to gain from a healthy ecosystem of both open source and proprietary COTS building block components. The benefits of using open source platforms such as Linux can help companies build security-rich, flexible, and scalable infrastructures, achieving levels of cost and time efficiencies crucial to accelerating development processes and speeding time to market. And the reuse of high-volume COTS components, which has long been a trend in enterprise, is now something the NEPs and service providers can leverage as more standardized COTS components designed for telecom are becoming available.

Key drivers

Let's look more closely at some of the key drivers for NEPs who are considering developing NGN solutions using COTS building blocks. What needs do these companies face that make them look for solutions that use building blocks from one or more vendors rather than build their own? The key drivers can be categorized into three distinct pressure points:

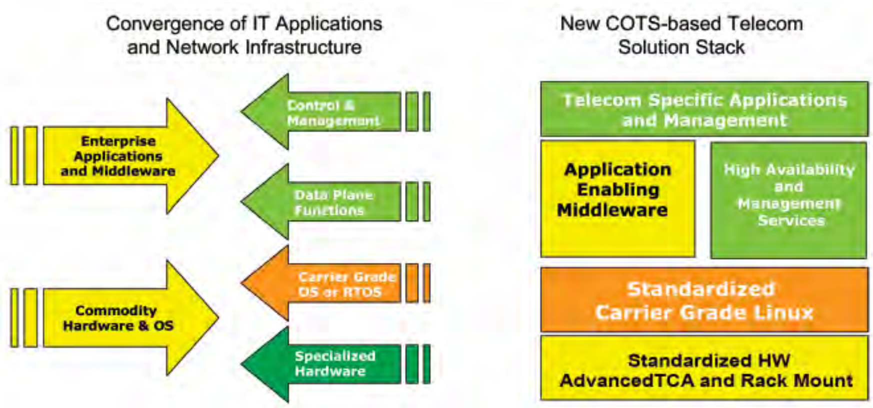

Figure 1

Consumer pressures
Service providers must simultaneously address customers' demands for increasing application complexity while delivering services at lower cost. At the same time advances in technology, especially the network, are driving demands for high bandwidth 24x7 services.

Business pressures
We still have the development cycles we inherited from the dot-com era, but not the financial exuberance. Service providers are expected to accomplish more and in less time, but for less cost than ever before. R&D budgets and operational costs are being slashed, yet at the same time providers must increase margins.

Competitive pressures
To add to the problems, in today's confusingly fast-paced business environment, product differentiation is more important than ever. The competitive field is stronger, and providers must get to market faster with better functionality than the competition.

One way that NEPs are relieving these pressures is by creating universal platforms that can be reused to build future products. This is where the use of reliable, commercial grade COTS components can provide significant cost benefits from building in-house solutions. Open source software enables leading edge technology and best-of-breed commercial solutions from ISVs and HW vendors. In addition, NEPs have access to all the functionality they need to develop state-of-the-art NGN solutions while also providing them with the control they need over their individual projects. Using these COTS-based platforms allows the NEPs to focus on their core value and still differentiate their products and services. These COTS-based universal platforms can then be reused for a multitude of NGN network elements, driving down costs and time to market.

Industry organizations driving COTS

Historically one of the challenges that NEPs face in achieving COTS solutions is the high cost and difficulty of integrating these COTS building blocks into reusable and interoperable components. In order for these COTS components to be truly reusable and interoperable, standards must be created to define the available services and the APIs that interface to those services. Many industry organizations have formed over the last few years to help grow and promote the ecosystem for COTS components being used in the telecommunications industry.

Open Source Development Labs (OSDL)
Recognized as the center of gravity for Linux, OSDL is dedicated to accelerating the use of Linux in all markets. OSDL is a key contributor to the COTS Telecom Solution Stack through sponsoring the Carrier Grade Linux Working Group. This is a group of Linux distributors, HW platform providers, and NEPs that are driving specifications for the standardization of a Carrier Grade Linux (CGL). Already in its second release, the CGL specification is the foundation of most COTS-based solution stacks being designed today.

PCI Industrial Computer Manufacturers Group (PICMG)
PICMG is a consortium of more than 450 companies who collaboratively develop open specifications for high performance telecommunications and industrial computing applications. Recently, PICMG announced the development of a new series of specifications, called AdvancedTCA, for next generation telecommunications equipment, with a new form factor, and based on switched fabric architectures. AdvancedTCA's success in the market has far exceeded initial expectations. Nearly every major NEP is planning AdvancedTCA-based NGN solutions.

Service Availability Forum (SAF)
The SAF goal is the adoption of open standards to enable the industry to build high availability network infrastructure products, systems, and services. The SAF is driving interface specifications to ensure high availability of services. As NEPs move towards a COTS model, they will need assurances that these new COTS applications will have the same level of services and availability as their legacy in-house solutions. The SAF is defining key services and the interfaces between the hardware platform, the operating system, and the High Availability (HA) middleware. The SAF is driving three key interface specifications:

- The Hardware Platform Interface Specification (HPI) defines the interfaces between the hardware and the operating system and middleware.
- The Application Interface Specification (AIS) defines interfaces for how HA middleware services communicate with each other and with the operating system. The AIS defines key services required for a complete HA system, including messaging, cluster membership, check-pointing, event monitoring, and frameworks.

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- Systems Management Specification (SMS) is a complementary specification that acts as an umbrella to tie together the already existing HPI and AIS specifications. It is an SNMP and Web-based interface specification that enables the service event and error reporting by AIS and HPI.

Each of these organizations (OSDL, PICMG, and SAF) are driving standards in key areas of the COTS solution stack. Figure 2 illustrates the areas where each standards effort affects the COTS solution stack. A significant amount of synergy and cooperation exists among these industry groups, for example the OSDL Carrier Grade Linux specification even specifies the SAF HPI and AIS interfaces as requirements for a Carrier Grade Linux operating system platform. The SAF is working with PICMG to ensure that the HPI interface is mapped to AdvancedTCA. While the CGL specification is designed to be hardware neutral, SAF is considering whether to include specific support for AdvancedTCA as well.

In the lower two layers of the telecom solution stack, Carrier Grade Linux combined with AdvancedTCA is becoming the de facto solution for telecommunications platforms and substantially lowers costs for all types of NGN solutions ranging from Radio Network Controllers (RNCs) and GPRS network elements to signaling and management servers. In the upper layers of the stack, for service availability and application services, there are more choices of third-party COTS components depending on the type of solution or application. It is in these layers that the SAF APIs for AIS and HPI are so important to drive standards to ensure interoperability and consistency in the services that are required across a multitude of solutions.

The role of open source and Carrier Grade Linux

Carrier Grade Linux has a unique role in the telecom solution stack because Linux is typically the only component that is based on open source. True, commercially available middleware products above the operating system are based on open source, such as databases and HA solutions, but these products do not have a dominating position in the COTS solution stack the way that Carrier Grade Linux does. There are significant benefits for the NEPs that are driving the adoption of Carrier Grade Linux into the new COTS-based architectures:

- Lower development costs by using commercial CGL rather than developing in-house
- Faster time to market by focusing resources on value-add and using COTS components where possible
- Reliability by getting commercial grade quality with tested and mature CGL distributions
- Leading edge functionality found with Linux that is not available in more proprietary operating systems
- Control of projects and no vendor dependency; flexibility to own the source and change vendors if necessary
- Scalability and flexibility of CGL that can be reused for multiple NGN solutions
- Long-term viability and road map from a commercial vendor

Because of the unique requirements of the telecom industry, Carrier Grade Linux was designed from the beginning to include functionality for the telecom industry that isn't found in typical Enterprise Linux distributions. One key example of this is the area of real-time technology. While the new Linux 2.6 kernel has made significant advances in mainstream real-time support, some CGL distributions include even stronger real-time support than what is available from mainstream Linux. Carrier Grade Linux distributions are beginning to reach the realm of RTOS and include hard real-time with such technologies as priority inheritance and user-space prioritization. But true to the nature of Open Source and Linux, these real-time enhancements are not *forks* or fragmentation, but rather formal open source projects that are optional modules or extensions to the standard Linux kernel.

Other areas of differentiation between CGL and Enterprise Linux are in service availability and high availability. For example there is activity in the open source community for both the SAF HPI and the AIS specifications. Both have launched successful open source projects, OpenHPI and OpenAIS respectively, which are gaining traction and are being adopted by Carrier Grade Linux distributors and other vendors creating open source solutions. Other examples of open source projects for high availability include such projects as redundant networking and safe disk unmounting in the case of failover. These are all examples of open source projects that can be found in some of the Carrier Grade Linux distributions available today that differentiate Carrier Grade Linux from its enterprise cousin. For the telecom solution stack, Carrier Grade Linux can now be used in both environments providing even higher levels of reuse and reduced costs. Carrier Grade Linux is robust enough to support the enterprise-based service applications and has the reliability to serve the network infrastructure.

The majority of new NGN products being designed by NEPs today are based on some form of Carrier Grade Linux. As many as five different Linux distributors claim to have a Carrier Grade Linux

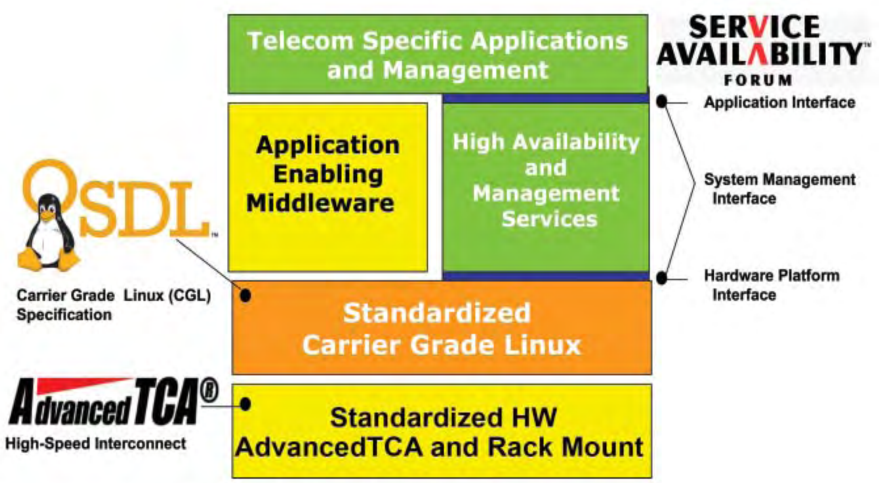

Figure 2

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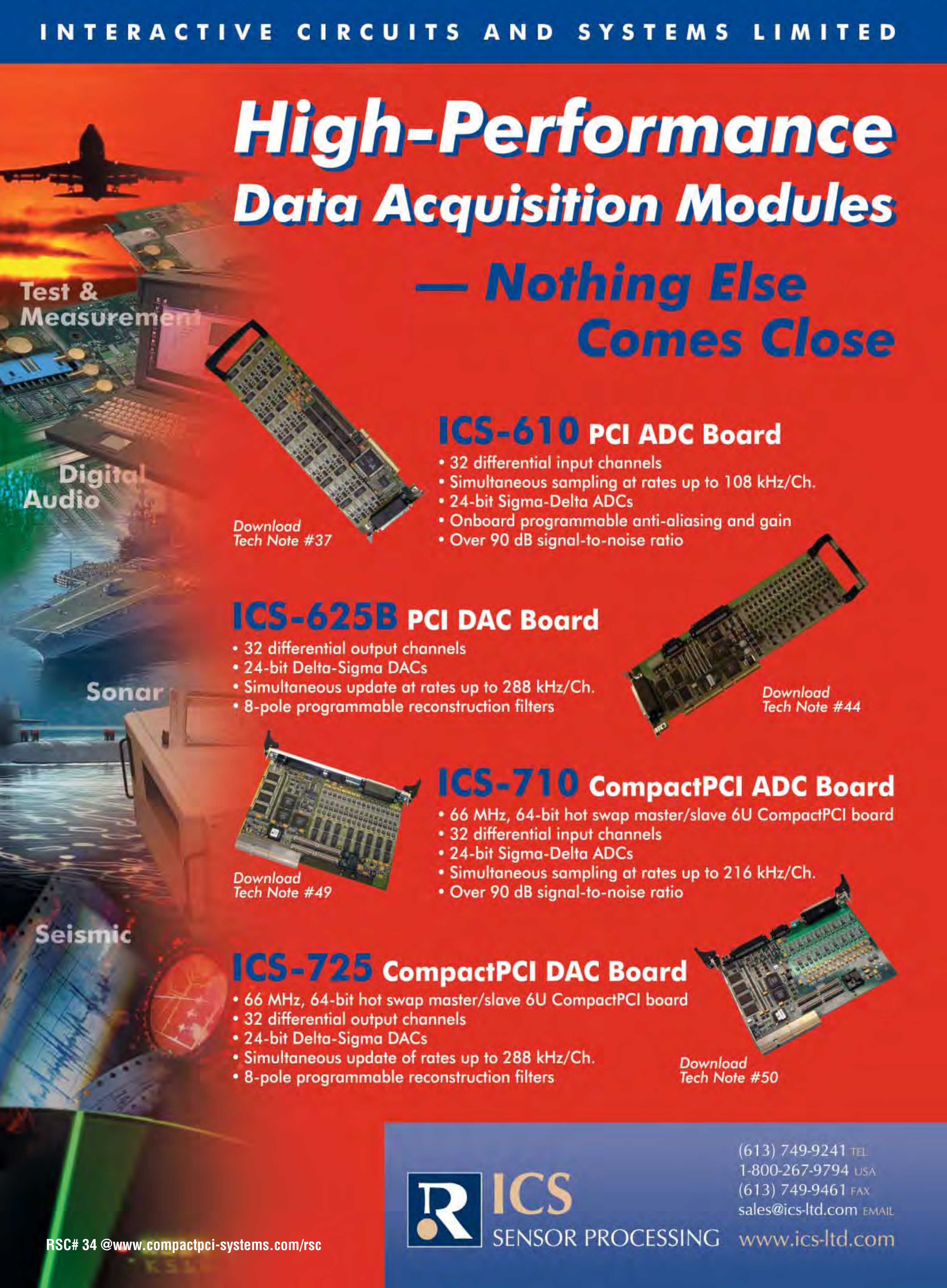
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offering. As of this writing, three Linux distributors have already registered their products on the OSDL website. NEPs now have many choices for delivering a Carrier Grade Linux operating system. Because Linux is Open Source and the CGL specification is available to anyone, NEPs always have the choice of developing their own Carrier Grade Linux product. But remember a strong driver of COTS is reducing operational expenses, including the R&D budget. While developing their own Linux distribution may seem attractive initially, nearly every major NEP has done the analysis and determined that the cost of integrating the various technologies included in the CGL specification, maintaining this code, and upgrading the distribution over time undermines the benefits of leveraging a COTS-based solution and far outweighs the costs of purchasing software and services from a commercial Linux distributor. Using a commercial Carrier Grade Linux distribution as the cornerstone of a COTS strategy for new NGN products enables NEPs to leverage the benefits of COTS to reduce costs and speed time to market while focusing on their value-added service.

***Glenn Seiler** is Director of Product Marketing for MontaVista Software and is responsible for managing MontaVista's Carrier Grade Linux strategy. In addition to his work at MontaVista, Glenn was also responsible for managing HA Clustering solutions at SCO. Glenn has more than 15 years experience managing UNIX and Linux operating systems including previous work with Texas Instruments, SCO, BSDi, and MontaVista Software.*

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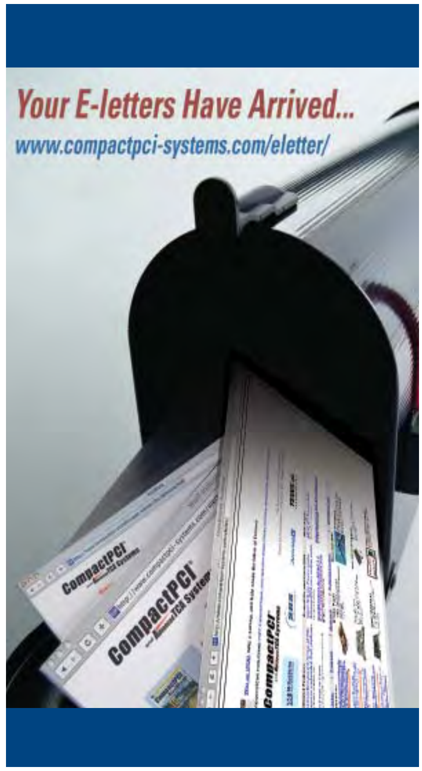

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PCI Express enables high-end embedded computing applications

By Jim Ison

Embedded computing has various meanings to each company designing products for the "embedded" computing market. For every definition of "embedded" there is a definition of what is considered "high-end." One thing typically remains the same when "high-end" and "embedded" are used together… there is never enough processing power to be considered "high-end" while remaining physically or thermally small enough to be considered "embedded." This is especially true when companies choose to adopt industry standard architectures based on widely available commercial desktop silicon. The form factor may not fit the application, or the high-end computing power may be overly constrained by the thermal requirements.

As PCI Express continues the imminent replacement of PCI as the host add-in card bus of choice, high-end embedded computing applications are poised to take advantage of this quantum leap in technology through several industry standards. Many of these standard architectures from the PCI-SIG, PICMG, and VITA organizations are pending release in the coming quarter. These standards will aid the embedded designer with a multitude of issues associated with high-performance embedded computing. In this article, Jim explains new technological advancements of the PCI Express bus that will enhance the architecture choices of high-end embedded computing designers. The standards discussed in this article include PCI Express Cable, COM Express, and CompactPCI Express with an overview of SHB Express, XMC, and MicroTCA.

PCI Express, in the most basic sense, is *packetized* PCI transmitted serially over several transmission media. The media can be traces inside a backplane, motherboard, or add-in board, or over a twisted pair cable in many standardized mechanical form factors. It is ideally suited toward high-speed chip-to-chip, board-to-board, and box-to-box applications. PCI Express uses Low Voltage Differential Signaling (LVDS) to transmit the PCI packets over, in the most basic form, a four-wire bus running at a clock speed of 2.5 GHz. This four-wire bus is referred to as a PCI Express lane. The lane provides a total available bandwidth of 5 Gbps. A single lane between two PCI Express end point devices, along with any of the optional sideband signals for enhanced features, is called a x1 *(by one)* link. Designers can place several lanes between PCI Express end points in parallel to achieve higher bandwidth links of x1, x4, x8, and x16, yielding a range of 5-80 Gbps of total bandwidth. Recent PCI Express press releases by the PCI-SIG plan on doubling the clock rate of second generation PCI Express (Gen2) to 5 GHz beginning in 2006. That would yield data rates of 10-160 Gbps late next year.

In addition to the hardware portion of the specification, PCI Express is inherently backward compatible with PCI in regards to operating system and application software. This compatibility allows the application and driver developer to use the same software tools used to develop PCI-based software. This is in contrast to the add-in card change from ISA/EISA to PCI that required new tools and operating systems.

PCI Express Cable

The first architecture to aid in high-end embedded applications is a PCI compatible cable expansion/extension capability based on PCI Express. PCI Express Cable is a standard undertaken by the PCI-SIG to transmit the host PCI Express bus over a high-speed cable. This can be done internal to a system enclosure or external in a box-to-box type application. Using a cable as shown in Figure 1, it is possible to extend the PCI Express bus approximately six to seven meters from the host CPU complex without the need for active equalization to suppress the inherent noise.

Figure 1

This particular cable is a x8 PCI Express external cable from Molex capable of transmitting 40 Gbps of data plus the PCI-SIG defined sideband signals.

Transmitting the host bus over copper cables opens a new world to the embedded designer. The PCI Express Cable enables a high-end computing core in a cooler area of a machine to host embedded I/O subsystems in remote, thermally constrained areas of the machine. The host and I/O system can be of different form factors suited to the location or performance each system requires. For example, a high-end, dual Intel Xeon class host system could provide the computing power for an operator interface and a high-speed data link to a high-end embedded I/O subsystem based on MicroTCA, PC/104, 3U CompactPCI Express, or proprietary form factor.

A compelling application of PCI Express Cable includes an expansion system, a set of products that extends the host bus of a system an arbitrary distance from the host enclosure to an expansion enclosure. This approach enables designers to insert more add-in boards into the system than the host system was originally designed for. A simple example of an expansion system is using a host interface board, cable, and 19-slot expansion chassis to extend a 4-slot ATX motherboard host system to a 20-slot system. Expanded systems in excess of 100 add-in boards are likely possible utilizing PCI Express expansion.

PCI Express Cable has a unique advantage over other expansion systems currently on the market. With PCI Express acting as

both the host bus and the cabled expansion protocol, it does not require drivers or conversion from the host bus to the expansion protocol then back again. This eliminates a root cause of some of the throughput latency of the expansion link. PCI Express offers a level of software compatibility and performance scalability unparalleled in even the most modern generation of cabled expansion systems currently on the market.

Other embedded applications for the PCI Express Cable are found across virtually all embedded markets. For example a high-speed docking station link for a high-end handheld or portable device useful in medical services, inventory control applications, or commercial laptops could employ PCI Express Cable. Another architecture a cabled solution could address is a noncontinuous backplane. This could take the form of several small backplanes in a nonconventional configuration, such as arranged in a circle or around a corner. In more traditional applications, an internal cable can replace the riser card of a 1U server where the add-in cards are mounted perpendicular to the motherboard.

COM Express

Another important standard is COM Express, which packs powerful PCI Express computing cores in small form factors for the embedded systems designer. COM Express is a PICMG effort to standardize PCI Express implementations of Computer-On-Module technology. COM Express standardizes two separate form factors and several different pin-outs, offering a choice to embedded developers.

Important features of COM Express include:

- Processor architecture independent
- Support for Gen1 and Gen2 PCI Express with two impedance controlled connectors
- 125 mm x 95 mm x 18 mm and 155 mm x 110 mm x 18 mm form factors
- Support for up to 32 lanes of PCI Express in several configurations
- Support for hybrid modules with a combination of PCI Express/PCI pin-outs
- Support for high-speed serial I/O and legacy parallel I/O
- Up to 160 W power budget per module

These modules allow embedded system designers to focus their core competencies on a carrier card that includes only the custom I/O functions required of the application. The designer can then attach the COM Express computing core module to the carrier card to form a customized embedded single board computer. The form factor and capability of the module proves useful in designing high-end handheld devices, custom shape carrier boards, and customized I/O carriers. The computing core of the carrier can be easily scaled to the application or upgraded with a new plug-in module, protecting the design from obsolescence.

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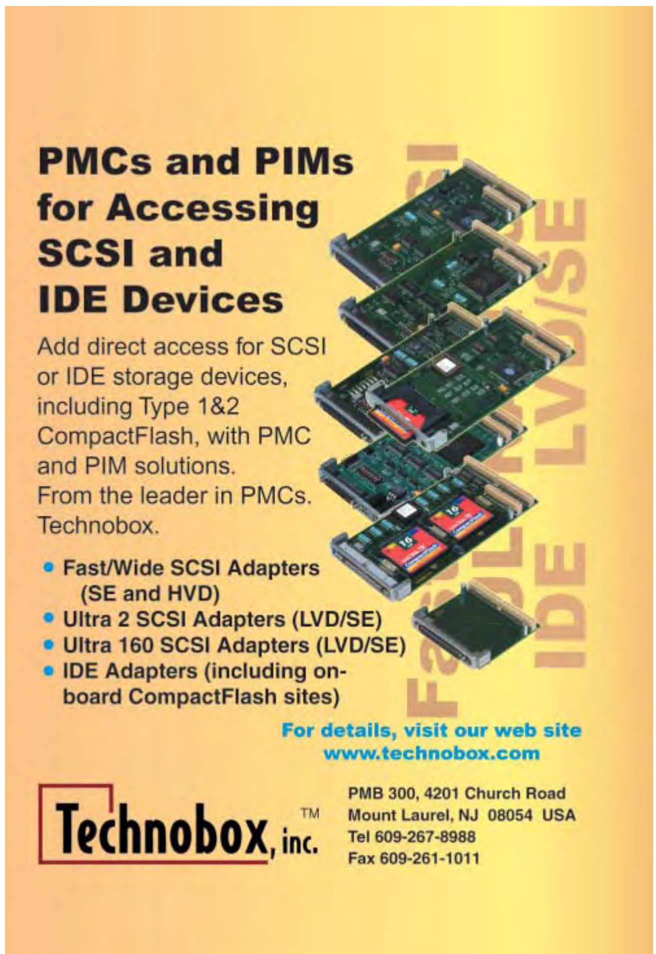

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Several PICMG member companies have announced COM Express modules and road maps. Figure 2 shows PFU Systems' basic form factor COM Express module.

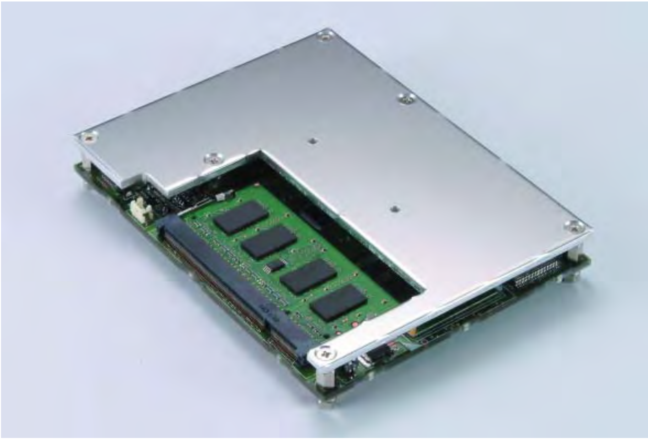

Figure 2

CompactPCI Express

For the embedded systems larger than a handheld device the CompactPCI standard has undergone a transformation to CompactPCI Express. CompactPCI Express is a PICMG standard pending release in the second or early third quarter of 2005. The base standard, named PICMG EXP.0:

- Improves power delivery to individual CompactPCI Express cards
- Supports Gen1 and Gen2 PCI Express bandwidth with an improved connector
- Includes provisions for CompactPCI/CompactPCI Express hybrid systems

Base features of CompactPCI, such as user I/O pins, rear I/O transition modules, support for telephony buses, and base mechanicals remain in the CompactPCI Express standard. This means for a 6U CompactPCI Express card the J3-J5 mechanical attributes remain the same as the base CompactPCI standard.

In contrast, the J1 and J2 of CompactPCI are replaced with improved connectors. Power delivery is achieved using a 7-pin Universal Power Module (UPM). The UPM is capable of delivering over 400 W of power to individual cards. The high-speed PCI Express interconnect is achieved with a 3-row Advanced Differential Fabric (ADF) connector. Two ADF connectors are used to provide up to 120 Gbps of available PCI Express bandwidth with to the backplane. A mini enriched 2 mm hard metric (eHM) functions in several capacities depending on the slot in which it is used. The eHM is a keyed connector that can provide rear I/O in 3U card form factors, power to low power (<34 W) cards, PXI trigger signals, or geographical addressing. Switch cards, used to support larger numbers of CompactPCI Express cards through fan-out, have a five-position UPM and a card edge filled with ADF connectors to maximize the fan-out to additional PCI Express slots.

Early manufacturers of embedded systems utilizing CompactPCI Express expect to leverage the wide array of available 3U and 6U legacy CompactPCI and PXI I/O cards. This is accomplished with readily available CompactPCI chassis and newly designed hybrid CompactPCI Express/CompactPCI system backplanes. The placement of switches and bridges can include direct backplane integration, rear pallet bridges, or slot loaded switch/bridge cards. Hybrid systems with CompactPCI Express and CompactPCI from One Stop Systems are now entering the market.

SHB Express

System Host Board Express is the passive backplane PICMG 1.3 specification. SHB Express defines a new PCI Express host single board computer form factor to support the passive backplane PCI/PCI Express market.

Features of SHB Express include:

- 20 lanes of PCI Express and a PCI-X bus on the card edge connector
- A dedicated connector for USB, Ethernet, and Serial ATA routing to the backplane to reduce cables to the SHB host
- Increased power capability to the host board to support higher performance processors

Embedded systems based on SHB Express range from "shoebox" style systems to 1U servers less than 17 inches deep. These form factors prove useful in embedded machine control, SCADA systems, computer telephony, and military communication applica-

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tions. The processing power of such systems currently reaches dual Xeon capability from One Stop Systems and other PICMG members.

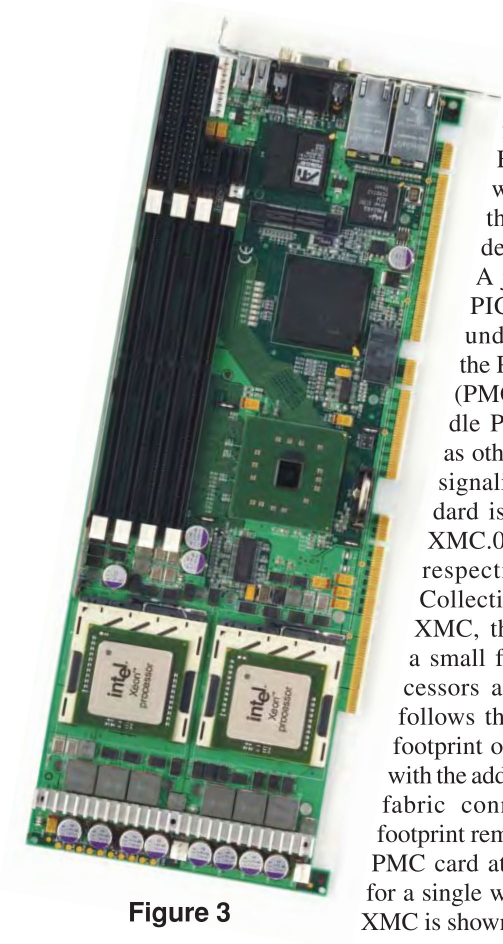

Figure 3

XMC

Several other small form factor PCI Express architectures will prove useful to the high-end embedded system designer. A joint effort between PICMG and VITA is underway to upgrade the PCI Mezzanine Card (PMC) standard to handle PCI Express as well as other high-speed fabric signaling. The base standard is known as PICMG XMC.0 or VITA 42 in the respective organizations. Collectively referred to as XMC, the standard defines a small form factor for processors and I/O boards that follows the exact mechanical footprint of the PMC standard with the addition of a high-speed fabric connector. The board footprint remains the same as the PMC card at 74 mm x 149 mm for a single width card. A sample XMC is shown in Figure 3.

A combination of XMC, PMC, and processor-enabled versions of these standards delivers benefits to the high-end embedded designer similar to those produced by CompactPCI Express or COM Express. XMCs are designed to enhance a CompactPCI Express system by adding functionality to a baseboard that is connected to an embedded backplane. Designers also utilize XMCs as standalone modules connected to a custom carrier card in an embedded system. Like COM Express, this carrier card can be application specific due to functionality or mechanical requirements. At 20 Gbps available bandwidth per XMC connector and with power consumption ratings from 7 W to 20 W, the XMC standard gives embedded designers a powerful tool.

MicroTCA

MicroTCA is a specification under investigation in the PICMG aimed at aiding the embedded designer. This specification is an extension to the PICMG Advanced Mezzanine Card (AMC) standard. AMCs are the mezzanine form factor of choice for the AdvancedTCA specification due to advanced features such as high-speed switched fabric, hot-swap, and IPMI system management support. AMCs accommodate both processor and I/O functionality. The board area of an AMC is roughly the same as a 3U CompactPCI Express card but has several choices of interconnect fabric including PCI Express, RapidIO, or Ethernet. MicroTCA aims to adapt the AMC mezzanine standard into a standalone, embedded architecture with a high-speed serial fabric interconnect.

Conclusion

PCI Express will become a valuable tool for the high-end embedded systems designer as the standards begin to release over the next few months. CompactPCI Express and MicroTCA embedded backplane based solutions offer a standard, modular, front plug form factor design option for high-end processors in small areas. XMC and COM Express offer mezzanine/carrier form factors for flexible baseboard design. PCI Express Cable reopens a chapter on cabled serial buses with higher performance than was possible with RS-232/422/485 or USB. In addition, PCI Express Cable can be combined with any (or several) of the other form factors to add an extra dimension to the architecture of the high-end embedded system.

The rewards of increased performance and flexibility coupled with the abundance of form factors available in PCI Express comes at the cost of some added complexity. With XMC and MicroTCA, manufacturers have the option of choosing serial fabrics other than PCI Express. Compatibility between modules with different fabrics must be considered. Also, several form factors have similar features and size that make for challenging architecture choices.

Systems manufacturers certainly must accept a more consultative role in overall system design with many new PCI Express architectures to choose from. The availability of off-the-shelf development systems that are application-ready, integration services based on standards based building blocks, and fast system turnaround times become critical factors in choosing a manufacturing partner.

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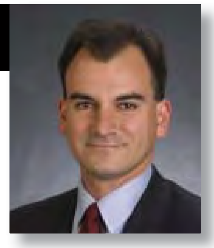
Using remote upgrades to increase revenue and decrease costs in wireless base stations



By David Gamba

The 3G rollout is now in full force and will be driving new data service requirements that will enable wireless operators to stem their ARPU decline. David argues that base station designs will need to offer more flexibility to meet the increasingly technically complex requirements for delivering next generation data services.

Though the 3G rollout has been delayed from original prognostications, the transition to 3G is moving very quickly now. According to iSuppli, 2004 marked the last year that any infrastructure dollars will be spent installing a 2G network, and 2006 will be the last year for any investment (and less than five percent at that) for a 2.5G network installation. The transition to 3G means associated higher speed standards can now be supported. The time is ripe for mobile operators to capitalize on the latest standards and quickly begin offering higher revenue generating data services to their customers. To this end, these operators can take advantage of a new flexible base station technology based on Field Programmable Gate Arrays (FPGAs) that enables in-field upgrades to support the latest industry standards and handset features. This flexible FPGA technology can also provide innovative ways to reduce operators' costs, helping increase profitability.

Wireless network evolution

As the Third Generation Partnership Project (3GPP) standards move from the 2G and 2.5G based standards of CDMA, GSM, GPRS, and TDMA to the 3G based standards of EDGE, CDMA2000, 1xDO-EV, and W-CMDA, new enriched data services and advanced functionality will be available. The enhanced revenue generating services will include messaging, photo transmission, e-mail, Internet access, motion video transmission, and e-commerce. What's more, advanced features such as Quality-of-Service (QoS) guarantees and bandwidth-on-demand adjustment capabilities will supplement these services, giving rise to more combinations of revenue generating packages for the wireless operators.

Reversing the trend of declining user revenue

The new data services and feature offerings will serve as a boon to wireless operators as they can now stabilize and reverse their eroding subscriber ARPU (see Table 1). This is especially important in regions with very high penetration rates such as Western Europe (79 percent), Japan (69 percent), and North America (58 percent), where new subscribers will not provide the growth necessary to drive revenues. In addition, by offering new data services and advanced features, wireless operators may be able to reduce their churn rate (especially in regions dominated by prepaid subscribers who do not have monthly contracts) by offering unique pricing packages.

Addressing technical requirements using remote upgrades

To enable these advanced data services offerings, the big question facing the wireless infrastructure industry is: What is the best way to deliver flexible, cost-effective solution deployments to meet these requirements? Given that the 3GPP standards are still evolving and that distinct geographical variations will exist for quite some time, wireless base station designs are incorporating more programmable technologies such as FPGAs in their designs. For example, the 3GPP Release 5 added a feature called High Speed Downlink Packet Access (HSDPA) as a new Universal Mobile Telecommunications System (UMTS) requirement in its baseband processing specification for Wideband Code Division Multiple Access (W-CDMA). This new feature enables base stations to transmit data to the handset units at a peak rate of 14.4 Mbps, a sevenfold increase over the previous downlink rate supported by Release 4 (2 Mbps). This performance increase enables more advanced data services that will help wireless operators raise ARPU. Adding HSDPA to the 3GPP standard required upgrading deployed base station units. Operators easily upgraded some base station designs by implementing an in-field upgrade to the FPGAs on the baseband card to add support for the HSPDA feature. Other designs, using inflexible ASICs, required either lengthy redesigns and verification efforts before respinning a new ASIC or a complementary device and baseband board redesign to support this new feature.

The HSDPA support issue offers a perfect example of how FPGA devices speed time-to-market product delivery and enable flexibility for field upgrades to support future standard changes or additions. Turning to FPGAs represents a long overdue shift away from using ASIC technology, which does not offer the ability to future-proof deployments against standards changes or the flexibility to support geographic customization.

Average Revenue Per User (ARPU)											
	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006
Voice	$82	$66	$54	$45	$39	$35	$33	$32	$31	$30	$29
Data	-	-	-	-	$1	$2	$4	$6	$8	$10	$13
Total	$82	$66	$54	$45	$40	$37	$37	$38	$39	$40	$42

Table 1

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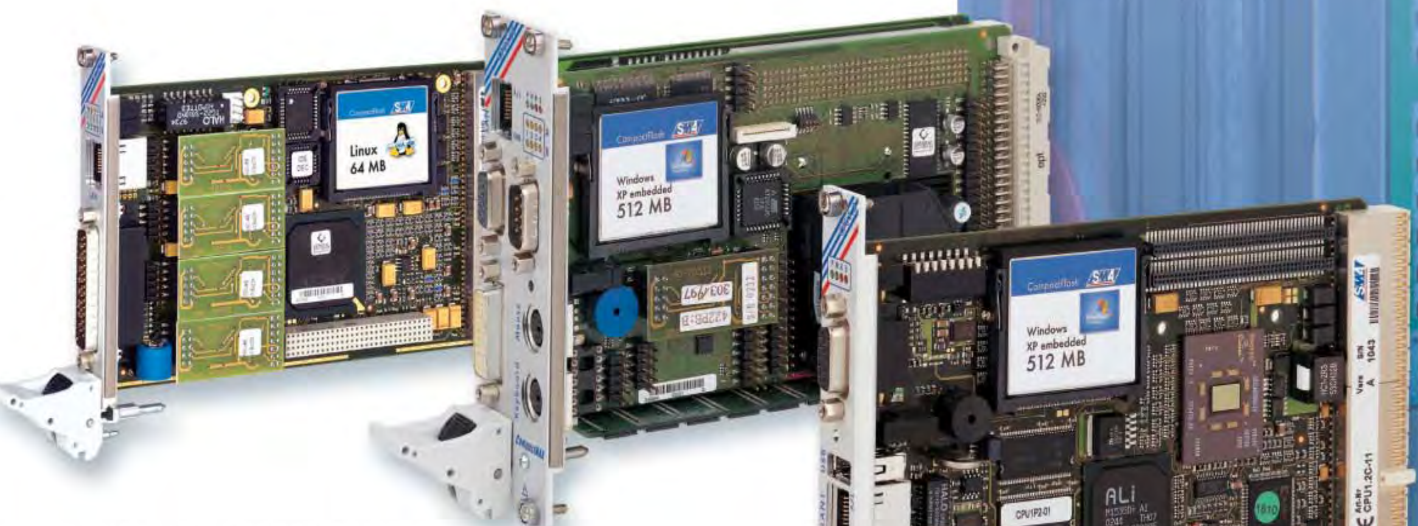

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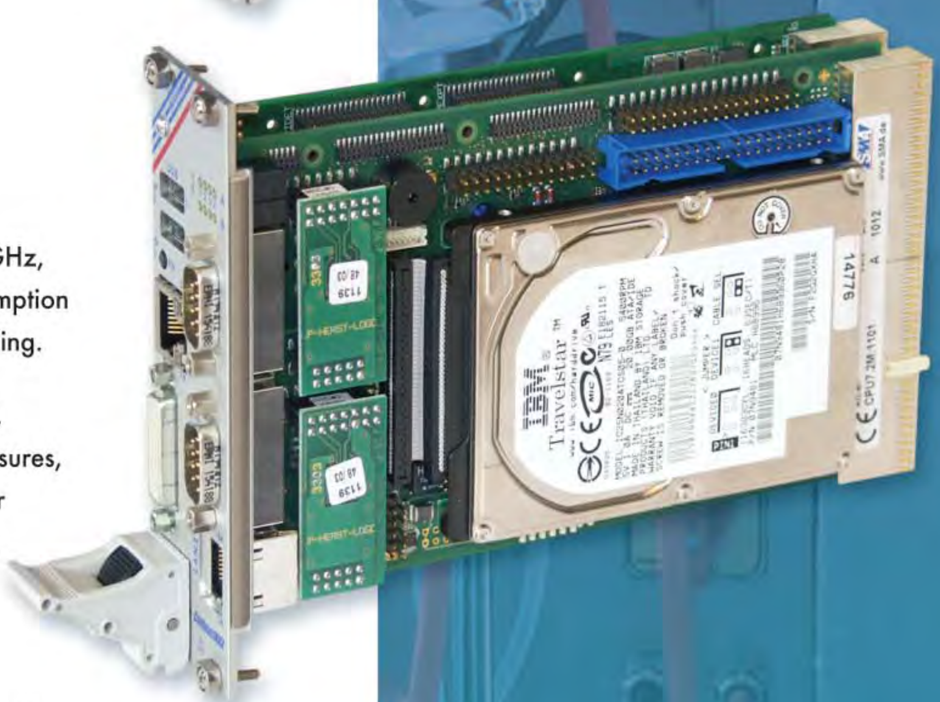

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For base stations implementing these new data service requirements, which support the higher speeds demanded by the downlink (HSDPA) and uplink (High-Speed Uplink Packet Access, or HSUPA, technologies coming in a future 3GPP release) speeds, baseband throughput, and processing power must increase. Processing power must grow to support the additional algorithmic requirements driven by the data service requirements and by an increasing number of users per base station. These design requirements dictate the use of components, such as FPGAs, that can effectively support single-chip parallel processing operations, as ASICs are not flexible enough for cost-effective deployment. Designers can effectively use FPGAs in the baseband modules of the wireless base station to implement the required performance levels. Using parallel processing techniques enables leveraging dedicated integrated signal processing functional blocks. These capabilities allow for flexible solutions that help reduce chip count and lower power inside the baseband module.

Reducing base station operating costs using programmability

FPGA programmability can also help significantly lower operating costs by offering operators increased power efficiencies during off-peak times. Wireless operators need to deploy enough base stations and remote radio antennas to support traffic loads during peak usage times. If the operator cannot support a handset user's request for a connection when the network is heavily loaded, then this service quality issue may drive the user to switch to another service. Thus wireless operators are forced to either sufficiently build out their own network to support peak loading times or rent enough usage time from an existing infrastructure to meet their peak loading needs. For reference purposes, a typical wireless base station network is depicted in Figure 1.

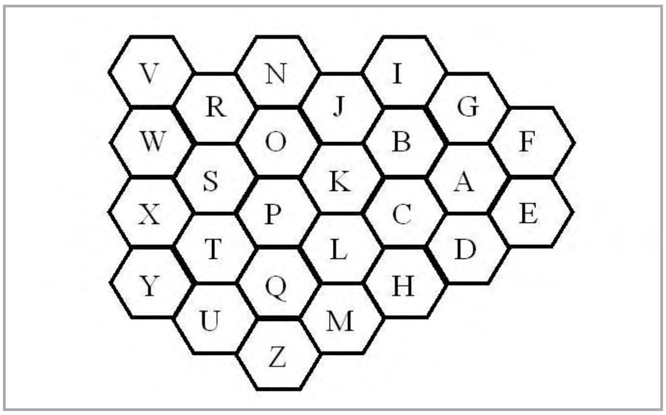
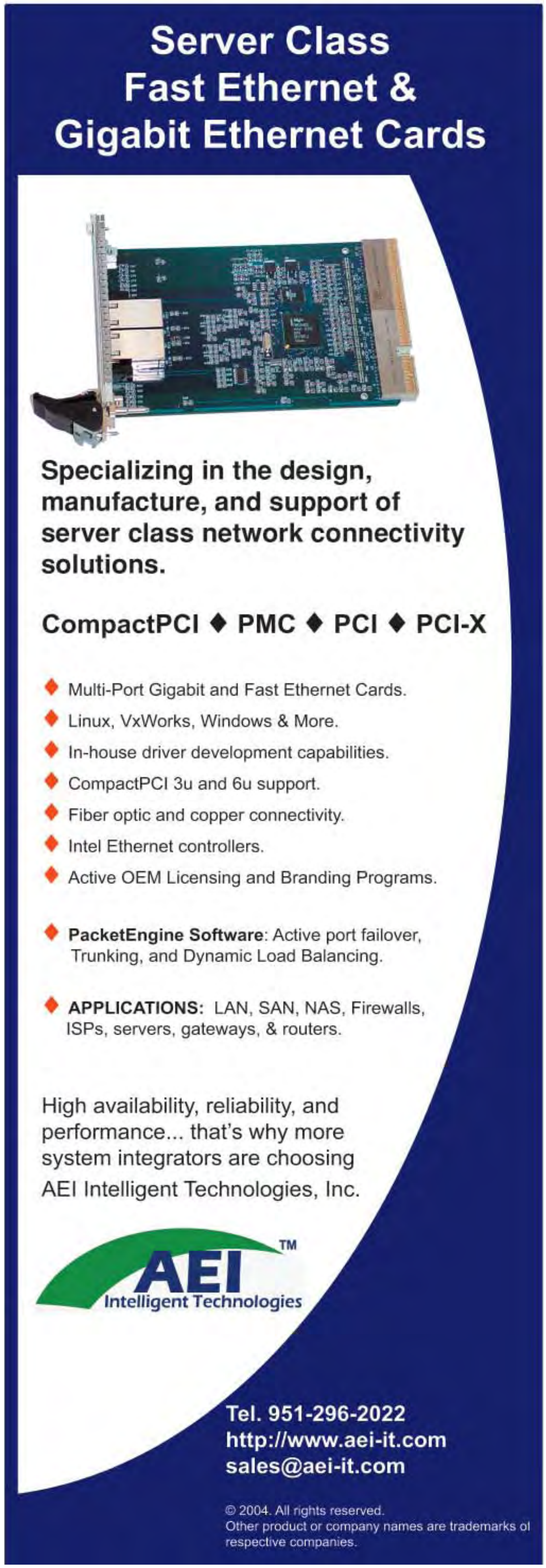


Figure 1

Not surprisingly, the traffic load on a wireless network decreases significantly during the late night and early morning hours. In certain locations, the traffic load also decreases on the weekends and holidays as well. This loading imbalance makes it possible for wireless operators to balance their network during this time. To successfully implement a power-balancing configuration, the wireless base stations must contain the flexibility to perform the following energy saving sequence:

1. Do not accept any new transactions.
2. Complete all existing transactions.



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3. Power down all unused sectors in the base station.
4. Maintain status monitoring to receive command status updates.
5. Power up when minimal load activity session activity lapses.

This type of flexibility is likely to be implemented in a staged approach in a real network, as one wireless base station after another is powered down (or removed from the network in the rental model) as the traffic load decreases, until a minimal configuration is reached. As an example, suppose that in the network shown in Figure 1 that 18 out of the 26 base stations can be powered down or removed from this network. This leads to a new network with the remaining base stations covering an expanded area as shown in Figure 2.

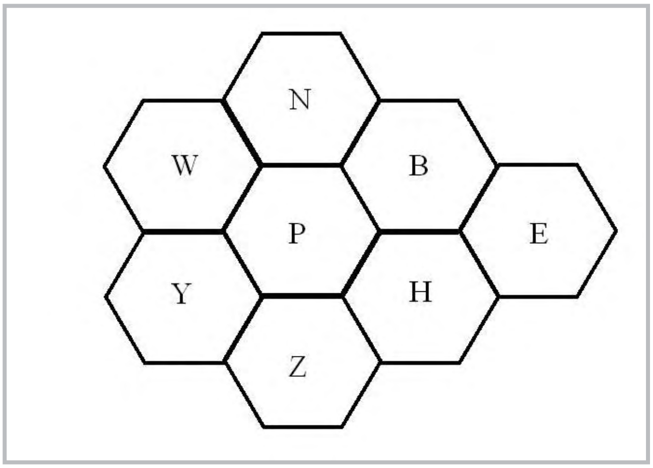

Figure 2

Powering down (or removing) these 18 base stations can provide a power savings in the network, helping lower the operator's operating expenses. To accurately estimate the power savings, one needs to note that the base stations remaining in the network will experience an increase in power due to base stations being removed from the network. The additional range needed to support geographical coverage for handsets formerly supported by base stations that have been removed from the network requires extra transmission power. Using an industry standard model presented in *Wireless Communications: Principles and Practices* [1] (and assuming an environmental factor of 2), the signal power required to travel across a distance *d* from a transmitter to receiver is described by Equation 1.

$$p_{ij} \sim (d_{ij})^2 \quad (1)$$

Equation 1

The significance of this model is that if the transmission distance is doubled by a factor of two, the power increases by a factor of four. However, this power increase is limited to the radio module of the wireless base station, which accounts for roughly 30 percent of the wireless base station power consumption. A quick power savings calculation reveals that the power consumption of the minimal network shown in Figure 2 will be a little under 60 percent of the peak load network shown in Figure 1, which allows for an over 40 percent power savings during the off-peak times.

Summary

3G will generate new data service requirements that will enable wireless operators to stem their ARPU decline. Given the constantly evolving wireless standards and the recognized need for geographic customization, programmable technologies are rapidly replacing traditional ASICs. This trend will continue as base station designs offer additional flexibility to address more and more complex technical requirements for delivering next generation data services. At the same time, base stations must maintain the versatility to avoid obsolescence or limited deployment by adapting to standards changes and geographic variations. In addition, these programmable technologies also offer operators an opportunity for cost savings by using the programmable flexibility to manage their networks through the service periods.

***David Gamba** is senior marketing manager for the Strategic Solutions Marketing Group at Xilinx. In this role, David is responsible for outbound marketing for all vertical markets supported by Xilinx solutions. David joined Xilinx in 2004 and brings more than eight years of experience in the semiconductor industry, where he served in a variety of marketing and sales roles including technical sales, product definition, and technical marketing. Prior to Xilinx, David held various positions at Aeluros, Conexant, and Altera. He holds a bachelor's degree in electrical engineering from UCLA, a master's degree in electrical engineering and computer science from UC Berkeley, and an MBA degree from Stanford University.*

References

[1] Dr. Ted Rappaport, *Wireless Communications: Principles and Practices,* 1996, Prentice Hall

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Just what is a *blade*, anyway?

By J. Eric Gulliksen

There is a tremendous amount of ambiguity surrounding the term "blade," particularly in the embedded space. It has become a marketing buzzword used to describe a variety of different product types, which has created confusion rather than differentiation in the marketplace. This article presents VDC's definition of the term, the logic behind this definition, and the ways in which we differentiate between blades and other embedded board types.

Beginnings

VDC first encountered the term blade during the course of research for our first report on *Switch Fabrics and High-Speed Serial Interconnects*, published in November of 2001. There appeared to be an intimate association between these interconnect technologies and the term *blade*. However, there was no clear definition for blades, blade architectures, or blade-based systems and, as the term became more widely used, this association with fabric technology started to become blurred. Definitions for *blade* found in various glossaries on the Web could be applied to Single Board Computers (SBCs) in general. We began to ask engineering and marketing professionals in both the embedded board and enterprise communities for their definitions in an attempt to arrive at a consensus. Some of the divergent responses we received from the embedded industry included:

- Just another, sexier word for *board*
- A board with some sheet metal wrapped around it
- A single board computer that has been optimized as a server
- The combination of a carrier board and a PMC card
- A PICMG 2.16 SBC
- An expansion card that plugs into a motherboard
- Another name for a 1U *pizza box* server

However, many of the other responses included an element of commonality, in that they *did* cite the use of high-speed serial or switch fabric interconnects as the primary means of interboard data communication. Discrepancies within this group were primarily related to the use of shared, parallel buses as additional means of interboard communication, or to functional types.

The Enterprise space showed a greater degree of clarity, although most Enterprise-class *blades* were of proprietary architectures or form factors. Here, the data communication means between *blades* was *limited* to high-speed serial or fabric interconnects, with little differentiation between functional types.

The VDC definition

Keeping these considerations in mind, VDC developed the following working definition for an embedded component-level *blade*.

An embedded component-level blade is a computer board with the following characteristics:

1. It is designed to be inserted, usually vertically, in a slot in a card cage or chassis mounted on a rack.
2. It connects to a passive backplane, and communicates data to other board level components in the immediate host system only via a switch fabric or other high-speed serial interconnect. Any shared, multidrop, parallel data bus that may be present is local to the blade and is not carried to the backplane.

We therefore base our definition on the structure of the interconnect architecture and do not limit it in any way by functional type, application, local bus, form factor, feature set, or any particular high-speed serial or fabric interconnect technology or topology.

VDC presented this definition to several of the individuals that we had previously interviewed, most of whom agreed that it made sense and provided much-needed clarity and differentiation between *blades* and boards using parallel buses as an interboard communication means. We then presented the definition verbally at the Bus & Board Conference in January of 2002, and it has now been accepted by a majority of the embedded board industry.

(Note that certain *blade servers*, which include 1U, 2U, and 4U devices, do not comply with provision 1 of this definition and may communicate with other blade servers via fiber or cable, without a backplane. We consider these to be system-level, not component-level, devices.)

Specifications

Of the various open standards in existence to date, only AdvancedTCA (PICMG 3.x) comprises a true *blade* specification. CompactTCA will also be a *blade* specification. Other standards such as PICMG 2.16 and 2.17 have provisions that allow, but do not mandate, blade configurations under the VDC definition. A CompactPCI single board computer example may help to clarify this gray area. Note that we will use the term *switch fabric* generically to include both fabrics and other high-speed serial interconnect means that may not be fabrics. In addition, the VDC definition allows for other functional types (such as I/O and mass storage) to be substituted for SBCs, and allows for *PICMG 2.16* and *Ethernet Fabric* to be replaced by other specifications and technologies, as appropriate. Thus, 2.16 may be replaced by 2.18 and *Ethernet Fabric* by *RapidIO*, for example.

"Traditional" CompactPCI SBCs *do not* include switch fabric access. Therefore, these *cannot* be *blades* under the VDC definition, and there is no ambiguity.

PICMG 2.16-compliant SBCs *do* include Ethernet Fabric access via the P0 connector. In other words, these are *fabric-enabled.* Fabric-enabled SBCs *may or may not* be *blades*, depending on their configuration:

- If these SBCs carry *both* the shared PCI bus and the Ethernet Fabric to the backplane as is permitted by the specification, these are *not blades.* We call these *nonblade fabric-enabled SBCs*. These configurations allow backward

compatibility with legacy backplanes and systems.

- *If,* as is also allowed under the PICMG 2.16 specification, the shared PCI bus *is not* carried to the backplane, these SBCs *are blades* under the VDC definition.

Configuration	Shipment shares by percent of $ volume
"Traditional" CompactPCI	43 percent
Fabric-enabled nonblade SBCs	44 percent
CompactPCI CPU *blades*	13 percent

Table 1

What if a fabric-enabled PICMG 2.16 SBC is used with a *backplane* that *does not* have the capability of connecting to or carrying the PCI bus between boards? Does this make the SBC a *blade*? No. In this case, the board is still a fabric-enabled SBC, but it is being used as a *blade*.

Recent study findings on CompactPCI SBCs and CPU *blades*

VDC's newly published report, *Merchant Computer Boards for Embedded/Real Time Applications Market Intelligence Program, 2004: Volume V: Overview*, indicates that, to date and other than AdvancedTCA, the only standards-based blades available are of the CompactPCI local bus architecture and form factor. Table 1 shows the dollar volume shipment shares of CompactPCI SBCs, in 2004, segmented into the three configurations mentioned earlier.

As a whole, shipment shares of fabric-enabled SBCs, including *blades*, are expected to continually increase. The relationship between shares of *blade* and nonblade fabric-enabled configurations is, however, projected to remain relatively constant until the CompactTCA specification becomes finalized. Ultimately, shipments of CompactPCI CPU *blades* are expected to overtake those of nonblade fabric-enabled SBCs, with the latter becoming relegated to a transition architecture.

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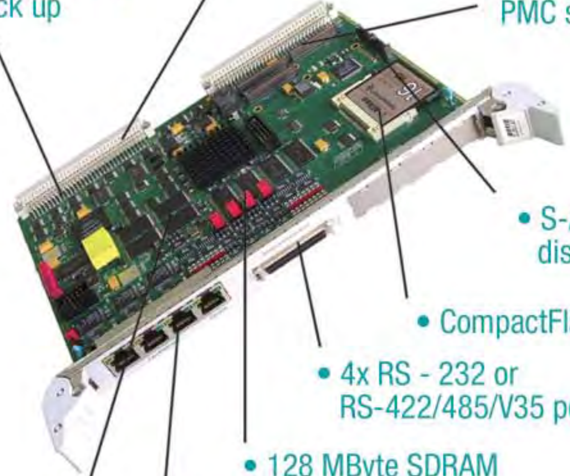

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Company name/ Model number	Processor				Features			
	Pentium III	Pentium M	PowerPC	Xeon	AdvancedTCA	PICMG 2.16	AMC sites	PMC sites
Acqiris www.acqiris.com								
PC502	•					•		
Actis www.actis-computer.com								
cSBC-6440			•					2
CSBC-6872Ax/144-16			•					2
ADLINK Technology www.adlinktech.com								
ATCA-6890				•	•			2
cPCI-3500A		•						
cPCI-3700A	•							
cPCI-3840 Series		•						
cPCI-6780	•							
cPCI-6810	•					•		2
cPCI-6820	•					•		
cPCI-6840		•						
cPCI-6860				•				
NuPRO-900				•				
Advantech www.advantech.com								
MIC-3351		•						
MIC-33513U		•						
MIC-3357		•						
MIC-3365	•							
MIC-3366	•					•		2
MIC-3369		•				•		
MIC-3385	•							
MIC-3389	•					•		
MIC-3369A		•				•		
Aitech www.rugged.com								
S950 Space Processor			•					
Artesyn Communication www.artesyncp.com								
BajaPPC 750			•					
Katana 752i			•			•		2
KatanaQp			•		•			
PM/PPC-750			•					
PmPPC7447			•					
Axiomtek www2005.axiomtek.com								
AXIOMTEK SBC83810		•						
Ballard Technology www.ballardtech.com								
OmniBus cPCI			•					

Company name/ Model number	Processor				Features			
	Pentium III	Pentium M	PowerPC	Xeon	AdvancedTCA	PICMG 2.16	AMC sites	PMC sites
Centralp Automatismes www.centralp.com								
KPCI6U-586PMC		•						
CES www.ces.ch								
Conduction Cooled RIOC 4070			•					2
MFCC 8442			•					
MFCC 8443			•					
MFCC 8447			•					
RIOC 4065			•					
RIOC 4068			•					
RIOC 4070			•					
RIOS 2476			•					
Cluster Labs www.cluster-labs.com								
CPU 410	•							
Computer Modules www.computermodules.com								
SC2060/SC2050	•							
SC2210	•							
Concurrent Technologies www.gocct.com								
2xPMC, Pentium M, SBC		•				•		2
PP 100/01x	•					•		
PP 110/01x	•					•		2
PP 120/01x	•					•		1
PP 120/11x	•					•		1
PP 220/01x				•		•		1
PP 312/012		•				•		2
PP 312/01x		•						2
PP 332/02x		•						
PP CP1/P3x	•					•		
PP CP2/P3x	•					•		1
PP EMB/P34	•							2
PP PSE/P31	•							1
PP SC2/P3x	•							1
Continuous Computing www.ccpu.com								
LINUXblade XE20				•	•			2
Curtiss-Wright Embedded www.cwcembedded.com								
G4C – cPCI SBC			•			•		
CompactCore '119			•					
DPMC-106			•					
PPC G4C			•					
SCP/DCP-122			•					

Continued on page 52

Company name/ Model number	Processor				Features			
	Pentium III	Pentium M	PowerPC	Xeon	AdvancedTCA	PICMG 2.16	AMC sites	PMC sites
Diversified Technology	www.dtims.com							
ATC-4130				•	•			2
DMD Computers	www.dmd.it							
DMD I815-C	•							
DNA Enterprises	www.dna-cs.com							
VS750			•					
Dynatem	www.dynatem.com							
CHC				•				
CPC2	•							
EKF-Electronik	www.ekf.de							
CC2-TANGO	•							
CC7-JAZZ	•							
CC9-SAMBA		•						
CCF-Concert	•							
CD2-BEBOP		•				•		1
ELTEC Electronik	www.eltec.com							
BAB 750			•					1
EUROCOM 248	•							
Eonic B.V.	www.eonic.com							
Atlas3-G4			•					
esd	www.esd-electronics.com							
CPCI-405			•					
EuroTecH	www.eurotech.it							
CPU-7630/7631	•							
CPU-7635	•					•		2
Extreme Engineering	www.xes-inc.com							
XPedite1032			•					
Fastwel	www.fastwel.com							
CPC501		•						
CPC502		•						
GE Fanuc Automation	www.gefanuc.com/embedded							
CPCI-7506		•						
PMC721TX			•					
VMICPCI-7505	•							
VMICPCI-7699		•						2
VMICPCI-7710	•							1
VMICPCI-7715	•							1
VMICPCI-7716	•							1
VMICPCI-7753	•							1
GE Fanuc Automation (continued)	www.gefanuc.com/embedded							
VMICPCI-7755	•							2
VMICPCI-7756	•							2
VMICPCI-7757	•							2
VMICPCI-7760	•							
VMICPCI-7761	•					•		1
VMICPCI-7806		•				•		2
VMIVME-7807		•						1
General Dynamics	www.gdcanada.com							
PC6010	•							1
General Micro Systems	www.gms4vme.com							
C161 Aurora	•					•		
C190/191 Atlantis-C			•					
C2000 Millennium	•							
C261 Aurora II		•						
C269 Equinox				•		•		
C394 Maverick			•					2
C50x Web-LC			•			•		1
CX269				•				1
Mariner II C158	•							
P60x		•						
GESPAC	www.gespac.ch							
PCIPPC-1			•					
PCIPPC-2			•					
PCIPPC-2X			•					
PCIPPC-5			•					
PCISYS-56AE		•						
PCISYS-58		•						
PCISYS-58X		•						
PCISYS-60	•							
PCISYS-PII/III	•							
I-BUS	www.ibus.com							
IBC 2600	•							
IBC 2601	•							
IBC 2602	•							
IBC 2801	•					•		1
IBC 2802	•					•		1
Inova	www.inova-computers.com							
ICP-(M)PIII	•							

Company name/ Model number	Processor: Pentium III	Processor: Pentium M	Processor: PowerPC	Processor: Xeon	Features: AdvancedTCA	Features: PICMG 2.16	Features: AMC sites	Features: PMC sites
Inova (continued) www.inova-computers.com								
ICP-CM/ICP-PM		•						
ICP-PIII	•							
ICP-PM		•						
ICP-PPC			•					
Intel www.intel.com								
NetStructure MPCBL0001				•				
NetStructure MPCBL5525		•				•		
NetStructure ZT 4807	•							
NetStructure ZT 5504	•							
NetStructure ZT 5515		•				•		
NetStructure ZT 5524	•							
Interface Amita www.interface-co.com								
CPZ-PE09 Series	•							
Kontron www.kontron.com								
AM4001		•						
AT8000				•	•			1
AT8001				•			2	
CP301	•							1
CP302-PM	•							
CP303	•							
CP304	•				•			
CP306		•						
CP320			•					
CP321			•					
CP6000		•				•		1
CP6010				•				1
CP6011		•				•		2
CP604	•							
CP620-PM			•					
cPCI-DMXS64	•							
cPCI-DT64	•					•		
cPCI-DXS64	•							
cPCI-MXP64GX	•							
cPCI-MXS64	•							1
cPCI-MXS64GX	•							
DT64	•					•		1
EB8245			•					
ETXexpress-PM		•						

Company name/ Model number	Processor: Pentium III	Processor: Pentium M	Processor: PowerPC	Processor: Xeon	Features: AdvancedTCA	Features: PICMG 2.16	Features: AMC sites	Features: PMC sites
Kontron (continued) www.kontron.com								
MXs64GX	•							
VisionCompact IA		•						
Maxwell www.maxwell.com								
SCS750			•					
MEN Micro www.menmicro.com								
A12c			•					
D3			•					2
D3a			•					
D3b			•					
D3c			•					
EM02	•							
EM04			•					
EM04N			•					
F1N			•					
F6			•					
F7	•							
F7N	•							
F9		•						
Mercury Computer Systems www.mc.com								
RACE++ 800 MHz PowerPC 7447			•					
RACE++ AdapDev	•							
RACE++ PowerPC 7410			•					
Microbus www.microbus.com								
MAT 1019	•							
Miriac www.miriac.com								
CPC45			•		•			
Momentum Computer www.momenco.com								
Cheetah-Cr		•						
Civet-C			•					2
Puma			•					
Puma-CR			•					2
Motorola www.motorola.com/computers								
ATCA Blade			•		•			
ATCA-715/717		•			•			4
CPCI-680			•					
CPCI-740		•						
CPCI-745		•				•		1

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Motorola (continued)								www.motorola.com/computers
CPV5370	•							
CPV5375	•							2
MCP750			•					
MCP820			•					
MCPN750			•					2
MCPN765			•					
MCPN805			•					
MPC8540 PowerQUICC III			•					
PowerCore CPCI-6750			•					
PowerCore CPCI-680			•					
PowerCore CPCI-690			•			•		
PowerCore CPCI-690+			•					
PowerCore CPCI-695			•					
PowerCoreCPCI-6750			•					
PPMC750			•					
PrPMC750			•					
MPL								www.mpl.ch
IPM6		•						
N.A.T.								www.nateurope.com
NICE-360					•			
National Instruments								www.ni.com
PXI 8176	•							
PXI-8175	•							
PXI-8175 RT	•							
PXI-8176 RT	•							
NEXCOM International								www.nexcom.com
MAXI 6600	•							1
MAXI 6750		•				•		1
One Stop Systems								www.onestopsystems.com
Millennium Gold			•					1
Orion Technologies								www.otisolutions.com
CPC7510			•					
PMC7500			•					
Performance Technologies								www.pt.com
CPC5505 PICMG 2.16 SBC		•						
ZT 5503 SBC	•							1
ZT 5504e SBC	•					•		1
Performance Technologies (continued)								www.pt.com
ZT 5515e SBC	•							
ZT 5524e SBC	•							
ZT 5551 SBC	•							
Portwell								www.portwell.com
TANC-5260				•	•			
Prodrive								www.prodrive.nl
P3P4403			•					
RadiSys Corp								www.radisys.com
Procelerant CE		•						
Radstone Embedded Computing								www.radstone.com
CP1A			•			•		
CP1A 6U			•					
IMP1A			•					
IMP2A			•					
Sanritz Automation								www.sanritz.co.jp
SC2050	•							
SBE								www.sbei.com
HW400C/M DKL			•					
SBS Technologies								www.sbs.com
C5C	•							
CC7	•							
CE7	•							
CK3			•					2
CK3-TM			•					
CK5			•					
CL9-cPCI 3U SBC		•						
CM4			•					
CP7	•							
CP9		•						
CR9		•						
CT7	•							2
CT8	•					•		
CT9		•						
RL4			•					
Siemens								www.siemens.com
CPCI-CPU076	•							

Continued on page 56

Company name/ Model number	Pentium III	Pentium M	PowerPC	Xeon	AdvancedTCA	PICMG 2.16	AMC sites	PMC sites
SMA www.SMAcomputers.com								
CPU 6.2	•							
CPU 7.2		•						
Smart Modular Technologies www.smartm.com								
SMARTengine/603ecPCI			•					1
SMARTengine/750cPCI-6U			•					
Spectrum Signal Processing www.spectrumsignal.com								
PRO-3500			•					
Synergy Microsystems www.synergymicro.com								
KGM5			•					
KYMD			•					
Technoland www.technoland.com								
TL-SBC 7450	•							
Thales www.thalescomputers.com								
CPU860-MD/MR/MM			•					
PMC860			•					
RA and RC PowerEngine7			•					
VMPC6a			•					
VMPC6c			•					1
Transtech DSP www.vmetro.com								
3CPF1			•					
CR9		•						
Trenton Technology www.trentontechnology.com								
CP10		•						1
CP16		•						
TriEMS www.triems.com								
TRL6227	•							1
United Electronic Industries www.ueidaq.com								
PDXI-C-P400/P700	•							
Voiceboard www.voiceboard.com								
PMC750			•					
VRose Microsystems www.vrosemicrosystems.com								
VRM-CC7-X	•							
VRM-CD1-X		•			•			1

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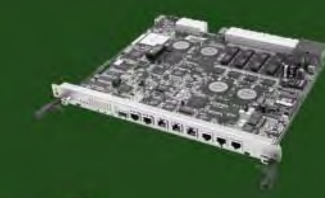

Diversified Technology's SBC Matrix

Board	Standard	Type	Processor/Ports	Features
ATC5231	AdvancedTCA	CPU Board	Single/Dual Xeon	ATCA 3.1, Intel E7520 Chipset, 800MHz FSB
ATC5232	AdvancedTCA	CPU Board	Single/Dual Xeon	ATCA 3.2, Intel E7520 Chipset, 800MHz FSB
ATC5234	AdvancedTCA	CPU Board	Single/Dual Xeon	ATCA 3.4, Intel E7520 Chipset, 800MHz FSB
ATC4130	AdvancedTCA	CPU Board	Xeon	ATCA 3.1, Intel E7501, 400MHz FSB
ATS1460	AdvancedTCA	Switch Board	ATCA 3.1 Option 4	High Availability, Base, Fabric ENET, FC Switch
ATS1160	AdvancedTCA	Switch Board	ATCA 3.1 Option 1	High Availability, Base and Fabric Ethernet Switch
ATS0020	AdvancedTCA	Switch Board	ATCA 3.0 switch	High Availability, Base Only Switch
ATS2148	AdvancedTCA	Switch Board	ATCA 3.2 Option 1	High Availability, Base and InfiniBand Switch
ATS1136	AdvancedTCA	Switch Board	ATCA 3.1 Option 1	Low Cost Base and Fabric Ethernet Switch
ATT001	AdvancedTCA	Test Board	Breakout and Test	ATCA Generic Fabric and Base Break Out Board
CPB4612	CompactPCI	CPU Board	Pentium M	Low Power, High Performance, Dual GigE
CPB4610	CompactPCI	CPU Board	Pentium M	Conduction Cooled, Ruggedized cPCI Blade
CPB4305	CompactPCI	CPU Board	Pentium 4-M	Low Power, Reduced cost CPU blade
CPB4321	CompactPCI	CPU Board	Pentium III	Low Cost, Lower Power
CPB4325	CompactPCI	CPU Board	Dual Pentium III	Dual Processor Blade
CSB4240	CompactPCI	Switch Board	Ethernet Switch	PICMG 2.16 Blade, packaged with PlexSys units
LBC9326	PCI/ISA	CPU Board	Single/Dual Xeon	LV Xeon, Intel E7520 Chipset, 800MHz FSB
LBC9017	PCI/ISA	CPU Board	Xeon	Low Voltage options, Dual GigE, ISA/PCI Bus
LBC9116	PCI/ISA	CPU Board	Pentium M	Low Power, 2.0GHz, 2MB L2 Cache, Dual GigE
LBC9216	PCI/ISA	CPU Board	Pentium 4/Celeron	Reduced cost, Multiple CPU performance options
LBC8940	PCI/ISA	CPU Board	Pentium III	Low cost, full-size PCI/ISA Card
LBC8540	PCI/ISA	CPU Board	Celeron	Low cost, full-size PCI/ISA Card
ETXLX15	ETX	CPU Board	Pentium M/Celeron M	Low power, Custom baseboard options
ETXLX05	ETX	CPU Board	Pentium III/Celeron	Low Cost, low power, Custom baseboard options
EPXL520	ePCI-X	CPU Board	Single/Dual Xeon	PICMG® 1.2, (2) Buses up to 64-bit/133MHz

Diversified Technology, Inc. (DTI) has a complete line of Rackmount Platforms and Systems that will help to package the perfect solution for your application needs. Visit our website to find out more information on what DTI can offer your company.

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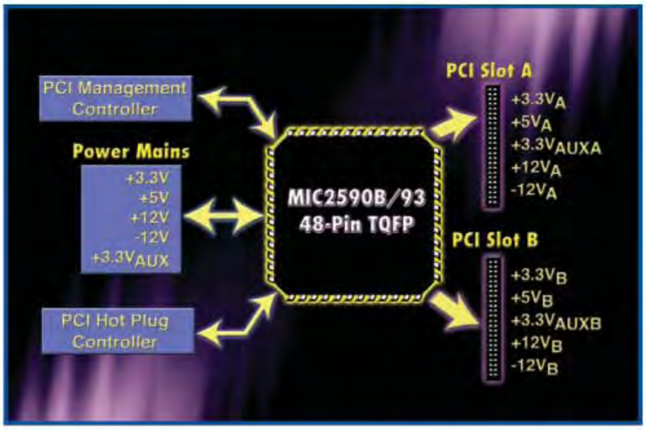
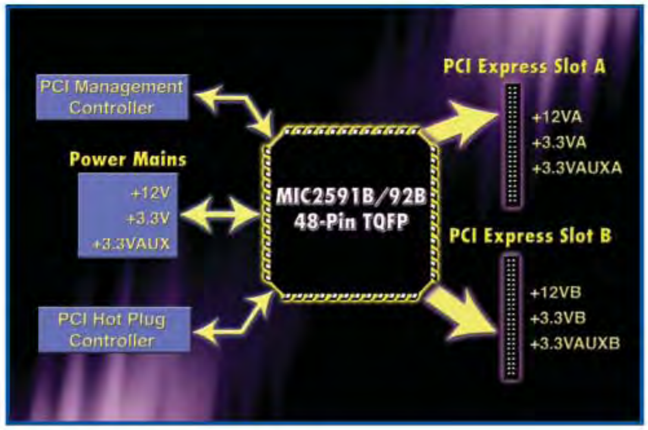
RSC# 57 @www.compactpci-systems.com/rsc

Introducing the Industry's Best-in-Class Dual-Slot Power Controllers

For PCI v2.x, PIC-X 1.0b/2.0 and PCI Express Applications



PCI v2.x and PCI-X 1.0b/2.0
MIC2590B/MIC2593



PCI Express
MIC2591B/MIC2592B

Micrel MIC259x family of multi-rail, dual-slot hot-swap controllers lowers overall system cost for implementing power controllers in PC board space conscious applications such as mid- and high-end enterprise server platforms. Micrel offers system design engineers one of four solution-optimized products that address dual-slot PCI v2.x, PCI-X 1.0b/2.0, or PCI Express power control requirements. For sophisticated power control and fault monitoring/reporting, all products incorporate an SMBus interface where the MIC2590B and the MIC2591B incorporate additional circuitry to support the Integrated Platform Management Interface (pursuant to IPMI v1.0).

For more information, please contact your local Micrel sales representative or visit us at: http://www.micrel.com/ad/mic259X.

MICREL®

www.micrel.com

Literature: 1 (800) 401-9572
Factory: 1 (408) 944-0800
Stocking Distributors: Arrow 1 (800) 777-2776
Future 1 (800) 388-8731
Newark 1 (800) 463-9275
Nu Horizons 1 (888) 747-6846

The Good Stuff:

- Compliant with PCI v2.x, PCI-X 1.0b, PCI-X 2.0 or PCI Express v1.0 power control requirements
- Support for two completely independent slots
- Programmable inrush current limiting with programmable timeout
- Dual-level, dual-speed overcurrent detection circuitry
- Slot power control with "Power-is-Good" and fault status reporting via:
  - An SMBus interface and/or
  - Dedicated hardware input/output lines
- Integrated gate driver circuits, current sense, & power MOSFETs
  - MIC2590B/93: +12V, -12V, and +3.3VAUX
  - MIC2591B/92B: +3.3VAUX
- Integrated high-side gate driver circuits for external MOSFETs
  - MIC2590B/93: +5V and +3V
  - MIC2591B/92B: +12V and +3V
- MIC2590B and MIC2591B Support IPMI v1.0
  - Integral analog multiplexer and 8-bit delta-sigma (Δ-Σ) ADC

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NEW PRODUCTS

By Chad Lumsden

www.compactpci-systems.com/products

CompactPCI & AdvancedTCA

ARINC

Curtiss-Wright Embedded

Website: www.cwcembedded.com
Model: P429A PMC **RSC No:** 20220
ARINC 429 communications controller • Complete ARINC interface • Multiple serial communications channels in a single PMC module • AMD 85C30 serial communications controller • DDC 00429/3282/3182 ARINC 429 solution chipset • Custom FPGA bridges the industrial standard PCI interface bus to these I/O devices and 4 Mbytes of Flash • Eight DMA channels, four for serial transmit and four for serial receive channels, to reduce the overhead processing of these serial channel by the processor on the host board • Separate FPGA provides redundancy logic, interrupt handler, watchdog timer, and an external pulse counter • Suitable for adding serial and ARINC 429 interfaces to the host processor board with an available industrial standard PMC slot

BACKPLANE

Carlo Gavazzi CS

Website: www.gavazzi-computing.com
Model: CompactPCI Backplanes **RSC No:** 20440
2-16 slots standard, 2-21 slots custom, and 6U (10-layer) or 7U (12-layer) format • CT bussing (ECTF H.110) • 5 volt/3.3 volt supported • ATX power supply connectors (7U format), power blocks (6U format) • PICMG 2.16 and 2.17 backplanes also available • Hot swap compatible


RSC 20440

ELMA Bustronic

Website: www.elmabustronic.com
Model: ATCA Backplanes **RSC No:** 20382
Controlled-impedance stripline design • Dual star, mesh, and replicated mesh configurations available • Slot size of 2, 5, or 14; both 5U and 7U heights available; other sizes available • Simulation/characterization studies confirm excellent signal integrity; unique AdvancedTCA probe card • Custom AdvancedTCA designs • Signal integrity studies

BACKPLANE: FULL MESH

Kaparel

Website: www.kaparel.com
Model: AdvancedTCA Backplane **RSC No:** 20385
14-slot fabric interface with full mesh interconnect • Base interface with dual star interconnect • Split power distribution (odd slots on A1/B1, even slots on A2/B2) • Bused IPMI-0 connections (optional configuration allows for radial connections) • Synchronization clock interface on P20 • Metallic test and ring generator buses on J10


RSC 20385

XILINX

Website: www.xilinx.com
Model: Xilinx ATCA Platform **RSC No:** 20387
Four-channel, four-port (16 MGTs) full mesh fabric interface • Supports IPMI interface and base interface ShMC port • Headers for application-specific personality module • Fully distributed system management architecture • Supports management firmware running on IBM PowerPC processor immersed in Virtex-II Pro FPGA family • Supports Linux-based control plane software


RSC 20387

BLADES: SERVER

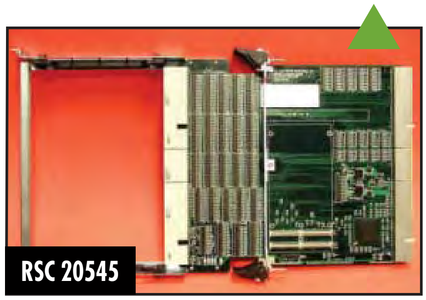
Diversified Technology

Website: www.dtims.com
Model: Targa-14 **RSC No:** 20421
14-slot AdvancedTCA communication solution for service providers and high-speed data network applications • Single/dual Intel Xeon processor-based node blades with speeds up to 2.8 GHz and 1 MB L2 cache • Separate data/control transfer accomplished via hub switch blades • MontaVista Linux Carrier Grade Edition (CGE) BSP for CPU node blades • Redundant management in either radial or bussed modes • Dual star and full mesh backplanes

BOARD ACCESSORIES

Zephyr Engineering

Website: www.zpci.com
Model: ZPCI.246 **RSC No:** 20545
Onboard bridge maintains CompactPCI signal integrity • Onboard PMC slot for PCI logic analyzer/exerciser • All CompactPCI and user I/O signals are individually isolatable • Supports PMC


RSC 20545

For further information, enter the product's RSC# at www.compactpci-systems.com/rsc

NEW PRODUCTS

user I/O on J3-J5 • Ideal for both CompactPCI and PMC board testing • Test points for all CompactPCI signals • Test points for all user I/O pins • Power test points simplify current measurements • Individual indicator LEDs show board power status at a glance • Rigid frame mates and locks with injectors on test board • 32-bit and 64-bit configurations available at 66 MHz • Short circuit protection for +3.3V, +5V, +12V, and –12V supplies

CARRIER BOARD: PMC

Technobox

Website: www.technobox.com
Model: 4366 **RSC No:** 20537
Adapts 32- or 64-bit PMC (33 MHz) for use in PCI slot • Designed for optimal signal quality • Support for rear I/O • LEDs convey status of key PCI bus signals and power • Accommodates external power • Optional fan assembly for additional cooling of PMC


RSC 20537

CHIPS & CORES: OTHER

Potentia Semiconductor

Website: www.potentiasemi.com
Model: PS-1006 **RSC No:** 20409
Extensive primary side monitoring delivered the PS-2406 across the isolation barrier via the PI-Link • -48V inrush control and timed circuit breaker functionality • Programmable sequencing for startup, shutdown, and fault conditions • Programmable output overvoltage (OV) and undervoltage (UV) warning and fault threshold • Three general-purpose analog inputs for monitoring temperature and other parameters

CONNECTOR: HARD METRIC

ERNI

Website: www.erni.com
Model: Ermet Connector **RSC No:** 20395
Fully compatible with 2 mm HM equipment • 2 mm HM hardware and accessories • Designed specifically for high speed differential • Optimized trace width and trace space • Supports speeds beyond 5.0 Gbps • 4-pair 25 mm provide 40 differential pairs/25 mm • 3-pair 25 mm provide 30 differential pairs/25 mm • 2-pair 25 mm provide 20 differential pairs/25 mm

CONNECTOR: MEZZANINE

Yamaichi Electronics

Website: www.yeu.com
Model: CN074 Series Connector **RSC No:** 20400
PICMG AMC.0 Revision 1.0 compliant • GR-1217-CORE compliant • Compression style contacts to the carrier board with wiping action to ensure high reliability • Integrated, high-performance Yamaichi developed YFlex with B²IT interconnect technology • Base substrate is LCP material, which has a very low CTE • Contacts designed for high-speed applications – very short stub • Supports speeds beyond 12.5 Gbps • Low Dielectric Constant Insulation Material: – Connector Housing: 3.10 @ 6 GHz – YFlex: 2.85 @ 6 GHz • Controlled impedance contacts 100 Ω+/-10Ω • 200 mating cycles • Operating temperature: -40 °C to +70 °C


RSC 20400

DEVELOPMENT PLATFORM

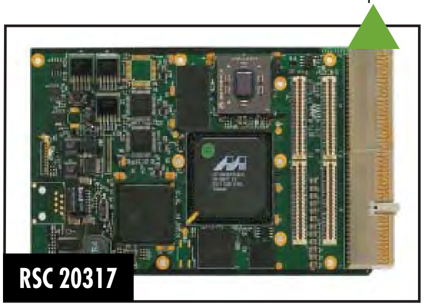
AudioCodes

Website: www.audiocodes.com
Model: TP-12610 SDK **RSC No:** 21266
2016 voice/fax LBR channels supporting multiple voice coders • Optional connectivity to 16 T1/E1/J1 PSTN trunks • Dual redundant Base and Fabric (3.1) interfaces • Fabric and base switch blade • Optional application processor blade • MGCP, MEGACO, SIP, and AudioCodes proprietary API • G.168-2002 compliant echo cancellation • Real-time fax over IP/T.38 • Wide selection of vocoders including AMR, EVRC, G.729, G.723, and G.711 • PSTN Signaling: CAS, ISDN PRI, and SS7 layer 2 termination • SIGTRAN IUA, M2UA, M3UA over SCTP • Tone detection and generation (MF, DTMF, RFC 2833) • Enhanced voice processing features including conferencing, voice detectors, and announcements

DSP RESOURCE BOARDS: COMPACTPCI

Mercury Computer Systems

Website: www.mc.com
Model: MCP3 FCN **RSC No:** 20317
A rugged, conduction-cooled 3U CompactPCI digital signal processing board • PowerPC 7447 @ 1 GHz • Virtex II Pro P40 FPGA Discovery II System Controller • Conduction cooled with options for air-cooled lab development • PMC site with additional general purpose direct-connected LVDS FPGA I/O • Designed for optimal performance with Mercury's dual-channel Analog to Digital Conversion PMC


RSC 20317

ENCLOSURE

Hybricon

Website: www.hybricon.com
Model: High Power Towers **RSC No:** 20452
Cooling up to 100 watts per slot • Eight-slot CompactPCI or VITA 1.7 VME64x switch fabric backplanes • High-quality construction in a lightweight portable design • Up to 800 watts of power • Front-access peripheral module with provisions for mounting CD-ROM, hard disk, and floppy drives • Custom configurations and integration services available

ENCLOSURE + CARD RACK + POWER SUPPLY

ELMA Electronic

Website: www.elma.com
Model: 12R1 COTS **RSC No:** 20566
A rugged chassis with shielding effectiveness • Weighs 20-25% less than Elma's previous models • Meets MIL-S-167, MIL-S-810E, MIL-S-461D, and MIL-S-901D standards • Holds 6U x 160 mm or 220 mm cards • Available in 22" and 25" depths or custom • Wide range of backplanes in up to 20 slot sizes is available in VME, VME64x, VXS, CompactPCI, or other architectures • Compliant to the IEEE 1101.10/.11 mechanical specifications • Front-to-rear cooling is achieved through a Rear Evacuative Cooling system often using 2 x 470 CFM Free Air Blowers • System monitoring LEDs for DC Voltages, over-temp, and fan fail standard • Includes convenient, separate front access to drives via a removable hinge door allowing space for drives (or Kingston carriers) • Large patch panel for I/O located on the rear of the chassis • 2 handles per side for easy lifting • Power supplies for up to 350-1400 W • Optional louvered front panel to meet the International Protection 53 code according to IEC 60529 for drip requirements • 2U to 9U heights in horizontal and vertical orientation • Modular design allows models to be developed in 2U and 3U heights • A clear alodine coating provides corrosion protection and an aesthetically pleasing finish • Designed to withstand the harsh demands of a military environment • Uses honeycomb filters, braided gasketing, and metal impregnated sheets to seal off all external seams


RSC 20566

• Withstands over 15 *g*'s of shock and vibration • Various options of rope-coil isolators, air springs, and elastomeric isolators are available • Suitable for making custom modifications quickly, easily, and cost-effectively

FABRICS: FIBRE CHANNEL

SANBlazeTechnology

Website: www.sanblaze.com
Model: PMC FibreChannel HBA **RSC No:** 20549
Two independent, 2 Gbit Fibre Channel ports • SFP based, supports multi-mode optics and copper options • Auto-negotiation for legacy connect (1 or 2 Gbit) • Front and rear panel I/O options; Pim Module available • Software supports switch and loop (private and public) topologies • 64-bit, 33/66 MHz PMC

FABRICS: INFINIBAND

Mellanox

Website: www.mellanox.com
Model: 10 Gb/s 24-Port **RSC No:** 20386
10 Gbps 24-port InfiniBand switch • 24 InfiniBand 4x 10 Gbps ports with Double Data Rate (DDR) 20 Gbps capability • Full-wire-speed capable switching core (960 Gbps) • Ports configurable into 12x uplinks (30 Gbps or 60 Gbps DDR) • Full, open-source Embedded Linux Management Kit available • Ideal for VXS VITA 41 or AdvancedTCA 3.2 backplane fabric • CPU interface for low-cost embedded fabric management

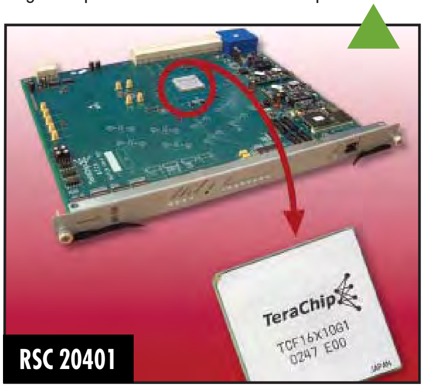
FABRICS: SWITCHED FABRIC

DSS Networks

Website: www.dssnetworks.com
Model: Model 8261 Switch **RSC No:** 20484
Fourth-generation BCM5690 switch fabric and BCM5464SRKB quad-port transceivers from Broadcom • High-performance wire speed on all ports – 24 Gb total; up to 32,000,000 frames per second maximum switching rate • Onboard firmware for configuration, management, and health monitoring • Cell and packet-based "head-of-line" blocking prevention; 1 MB of onboard memory for packet buffering • Extended Ethernet frame sizes to 9 KB; fully compliant to IEEE 802.3 specifications, including auto negotiation • Onboard Motorola DSP56F826, 80-MHz RISC/DSP processor for local management; serial port for console CL1 and debug

TeraChip

Website: www.tera-chip.com
Model: Switch Fabric Solution **RSC No:** 20401
AdvancedTCA compliant 160 Gbps solution • Single-chip based solution with low power consumption of only 15 W • Scalable up to 320 Gbps in an AdvancedTCA chassis • Switch card redundancy of 1:1 and 1+1 • Line card protection • Directed end-to-end Flow Control (FC) by slot and CoS • Dynamic load balancing • Dynamic cell size • 8 CoS queuing on ingress and egress with WRR & Strict priority



RSC 20401

FRONT-PANEL HARDWARE

Phillips Components

Website: www.phillipscomponents.net
Model: VME, CPCI Panels, PMC **RSC No:** 20460
VME panels and hardware • CompactPCI panels and hardware • PMC bezels • PCI brackets • Ejectors • Card guides • Custom molding

Tyco Electronics

Website: www.tycoelectronics.com
Model: Guide Hardware **RSC No:** 20384
Configurations for front board and backplane as well as mid-plane and coplanar applications in the RTM • Vertical and right-angle pins to support right-angle and coplanar board configurations • Guide pins are available in short or long lengths to accommodate various Tyco Electronics connectors

RSC 20384

NEW PRODUCTS

I/O: ANALOG

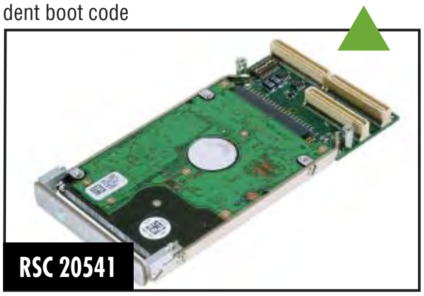
Parsec

Website: www.parsec.co.za
Model: PM488: Dual DAC PMC **RSC No:** 20533
Two Analog Devices AD9772A 150 MSPS 14-bit DAC converters • SNR of 70 dB @ 25 MHz and SFDR of 80 dB @ 5 MHz • 50 Ohm AC coupled analog outputs with 67.5 MHz reconstruction pass band • 32/64-bit 33/66 MHz 3.3 V PCI interface implemented in Altera Stratix FPGA • Internal data buffers of 16K samples per channel • Ideal for baseband or IF waveform reconstruction, W-CDMA, radar, and Software Defined Radio

MASS STORAGE: IDE

Technobox

Website: www.technobox.com
Model: 4170 **RSC No:** 20541
Provides a single Ultra160 SE/LVD interface • LSI 53C1000R controller • Front panel connectivity via 68-pin VHDCI connector with user-selectable active termination • Automatic setting of signaling mode, bus width, and clock • Front-panel status LEDs show bus activity, modes, etc. • Flash-resident boot code


RSC 20541

MASS STORAGE: PLUG-IN UNIT

SMA

Website: www.SMAcomputers.com
Model: CMASS7 **RSC No:** 20845
Mass storage module for the SMA Computers 3U CompactPCI CompactMAX CPU7.2 with Intel Pentium M processor

MASS STORAGE: RAID

SANBlazeTechnology

Website: www.sanblaze.com
Model: SB-SCSI Raid Blade **RSC No:** 20472
Single or dual SCSI drive options with SCSI Ultra320 support • In/out high-density SCSI connectors support daisy chaining with auto-termination • 36 GB to 146 GB of storage in a 6U, single-, or dual-slot CompactPCI form factor • Can provide RAID 0 (striping) and RAID 1 (mirroring) functionality • Hot swappable, IPMI support • Removable hot-swap drive version available


RSC 20472

MEMORY: FLASH

Aitech

Website: www.rugged.com
Model: S990 Memory Module **RSC No:** 20508
1 GB NAND Flash memory in four memory banks with 100,000 write/erase cycles • Hardware EDAC capable of single-bit error correction and multiple-bit error detection • Hardware has automatic power-off switch to latched-up memory to prevent damages from SEL events • Error detection, correction, and switch-off events are communicated via programmable interrupts to the CompactPCI bus • Flash File Driver (FFD) VxWorks software package to provide a file system with level-wearing features • Low power consumption of less than 3 W


RSC 20508

MEMORY: GENERAL PURPOSE

Virtium Technology

Website: www.virtium.com
Model: 2 GB DDR2 ECC **RSC No:** 20394
VM493T5653-CC/D5/E6 – DDR2 Reg. ECC 1.450" height, 0.150" thickness • VM491T5653-CC/D5/E6 – DDR2 Unb. ECC 1.450" height, 0.150" thickness • VM483L5625-B0/B3/CC – DDR Reg. ECC 1.400" height, 0.280" thickness, four-bank module with low-cost 512 Mbit ICs • VM485L5625-B0/B3/CC – DDR Unb. ECC 1.400" 0.280" thickness, four-bank module with low-cost 512 Mbit ICs • Rugged designs and BOM control • ECC/Non-ECC options

MOTION CONTROL

Pro-Dex/Oregon Micro Systems

Website: www.pro-dex.com
Model: CIX **RSC No:** 20476
One to four axis of Servo, Open Loop Stepper, or Closed Loop Stepper axis control options • Standalone with high-speed RS-232 port • 16 bit DAC analog resolution • Configurable PID filter with feed forward coefficients • Encoder feedback available for stepper axes • Two limits, one home, and one auxiliary output are standard per axis • Up to eight user definable I/O, expandable to 144 opto-isolated I/O • Constant velocity linear interpolation (all axes) • Software for Windows 98/NT/2000/XP • Electronic gearing • Circular interpolation • Linear, Parabolic, Cosine, and custom profiles

POWER SUPPLY

C&D Technologies

Website: www.cdpoweronline.com
Model: CPCI200A-1 **RSC No:** 20488
Active power correction • Complies with EN61000-3-2 • 90-264VAC input range • 3U x 4HP package • PICMG 2.11 compliant • Low airflow – requires as little as 200 lfm of airflow • Fault tolerant N+1 configuration • Output fault isolation

Picor

Website: www.picorpower.com
Model: QPI-6 Active EMI Filter **RSC No:** 20212
14 A rating • 80 VDC (maximum input) • 100 VDC surge 100 ms • >40 dB CM attenuation at 250 kHz • >80 dB DM attenuation at 250 kHz • -40 °C to +100 °C PCB temperature • Efficiency >99 percent at full load • 1,500 VDC hipot hold off to shield plane • 1.0" x 1.0" x 0.2" System-in-Package (SiP) • SMT Land Grid Array (LGA)

Wolf Industrial Systems

Website: www.wolf.ca
Model: SCAMP Power Panel **RSC No:** 20492
Eight individually protected and monitored 15-amp 125 VAC outlets; external alarm port; total current at 30 amps • Eight individual illuminated circuit breakers • Blue backlit LCD display of voltage, current, and power levels for total and individual circuits • Ethernet port for Internet or remote monitoring and control; serial diagnostic and configuration port • Time-stamped log of AC power quality • 15 ft. 30-amp FT4 rated cable with twist and lock plug • UL and CSA approved

RSC 20492

PROCESSOR BLADES

Diversified Technology

Website: www.dtims.com
Model: ATC5231 **RSC No:** 20125
Dual LV Intel Xeon with speeds up to 2.8 GHz and 1 MB L2 Cache • Intel E7520 Chipset • 800 MHz Front Side Bus • Supports one on-board 64-bit/66 MHz 3.3 V PMC cards • Two 10/100/1000 Mbps auto-negotiating Ethernet controllers for the base interface • Two 1000 Mbps Ethernet ports for the fabric interface • One 64-bit/66 MHz PMC site

PROCESSOR: PENTIUM 4

ADLINK Technology

Website: www.adlinktech.com
Model: NuPRO-850 **RSC No:** 20557
Socket 478 Pentium 4 processor, up to 3.4 GHz • Longevity Intel 875P chipset, 800/533 MHz FSB • Four dual/single-channel DIMM, maximum 4 GB DDR RAM, ECC or non-ECC support • AGP 8x

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Bus Structures
- CPCI/2.16
- AdvancedTCA
- VME/64x, VXS
- Custom

Standard Enclosures
- 19" and 23" Rack mount
- 1U to 14U
- 2 to 21 slots
- IEEE1101.10/.11
- STMP

NPI Solutions
- Design
- Prototype
- Testing
- Manufacturing
- Assembly
- Integration

Testing
- Shock and Vibration
- EMC
- NEBS
- Thermal Analysis

Certification
- FCC Class A, B
- UL, CSA, CE
- NEBS Level III

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NEW PRODUCTS

high-performance graphics • VGA, GbE, USB 2.0, IDE, S-ATA, COM, keyboard, and mouse • ePCI-X bus, miniPCI expansion slot

PROCESSOR: PENTIUM III

Carlo Gavazzi CS

Website: www.gavazzi-computing.com
Model: FabricPac Platform **RSC No:** 20456
2.16 Packet Switch-compliant, eight-slot backplane with CompactPCI, H.110, and IPMB buses • 8HP Intel Pentium III Processor SBC • Hard drive, CD, and floppy • Your choice of OS (Windows 2000, Windows NT, Linux, or Solaris) • Your choice of memory • Layer 2 or 3 switch card

PROCESSOR: PENTIUM M

GE Fanuc Automation

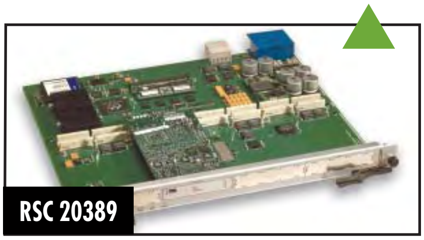
Website: www.gefanuc.com/embedded
Model: CPCI-7506 **RSC No:** 20301
3U CompactPCI Single Board Computer for multiple industrial automation and commercial applications • Intel Pentium M operating at speeds of 1.1 GHz, 1.6 GHz, and 1.8 GHz or Celeron M processor at 1.3 GHz • 400 MHz front-side bus • Internal SVGA controller via Intel's 855GME chipset • Up to 1 Gbyte DDR SDRAM • Dual Gigabit Ethernet interfaces • Two USB 2.0 ports • Two optically isolated serial ports supporting RS-232/422/485, one SVGA port, and a PS/2 connection • Rear I/O support includes one Gigabit Ethernet port, two additional USB 2.0 ports, two 16550-compatible TTL level serial ports, and a parallel port • Up to 1 GB of onboard CompactFlash or an onboard IDE hard disk drive • Support for one watchdog, two 16-bit, and two 32-bit software programmable timers • Operating system support includes Windows 2000, Windows XP, Linux, and VxWorks

RSC 20301

PROCESSOR: POWERPC

Artesyn Communication

Website: www.artesyncp.com
Model: KatanaQp **RSC No:** 20389
Single or Dual PowerPC MPC7447A processors running at up to 1.3GHz 2-Way SMP Architecture • AdvancedTCA PICMG 3.1 Node (1000Base-T Base Fabric + Octal High Speed GbE Fabric) Layer 2 or 3 • Ethernet switch option Quad PTMC expansion sites • Redundant System Management Bus with IPM • Controller Up to 2 Gbyte DDR SDRAM w/ ECC in SODIMM package Up to 128 MB Linear Flash • Real-Time Clock with supercap backup • VxWorks and CG Linux support • Quality assured by over 30 years of experience as well as ISO-9001 and TL-9000 certification



RSC 20389

PROCESSOR: XEON

ADLINK Technology

Website: www.adlinktech.com
Model: ATCA-6890 **RSC No:** 20390
One or two Xeon and next-generation Xeon processors, up to 3.67 GHz • Intel E7520 chipset, 800 MHz FSB • Four DDR II-400 240-pin DIMMs, 16 GB memory maximum • Two PMC slots with PCI-X bus with one supporting Jn4/Pn4 to RTM • Seven GbE data ports: Four fabric Interface and two base interface • One 10/100/1000Base-T management port (front panel) • ATI RageXL video • Two Serial ATA, two Parallel ATA, two Serial, and four USB 2.0 ports

Kontron

Website: www.kontron.com
Model: AT8001ATCA processor **RSC No:** 20392
Single slot AdvancedTCA PICMG 3.0/3.1 processor board • Intel Xeon processor, scalable up to 2.8 GHz • Dual AMC, one module support • Dual DDR-II DIMM for 8 GB of PC2-3200 registered 400 SDRAM • Dual Gigabit Ethernet base interface • Dual Gigabit Ethernet plus Dual Fibre Channel on fabric interface • IPMI v1.5 support

PROTOTYPING AND DEBUGGING: BOUNDARY SCAN

GÖPEL

Website: www.goepel.com
Model: SCANFLEX **RSC No:** 20808
JTAG boundary scan hardware • A complete modular system consisting of SCANFLEX Boundary Scan controllers (SFX-Controller) with external SCANFLEX TAP transceivers (SFX-Transceiver) and parallel controlled SCANFLEX I/O modules (SFX-Module) • Optional analog, digital, and mixed-signal channels can be directly added to the UUT interface • Support of up to eight parallel independent TAPs whereby each TAP is individually programmable in many parameters • 32 I/O lines for event control and 8 auxiliary I/O lines for additional analog and digital functions • There may be a 5 m distance between the SFX-Transceiver, typically without the need for a separate power supply or hardware controller

PROTOTYPING AND DEBUGGING: BUS ANALYZER

Fulcrum9

Website: www.fulcrum9.com
Model: Tx/Rx BenchBlade **RSC No:** 20405
AdvancedTCA compatible design using the right angle male HM-ZD connector for bench testing AdvancedTCA hub and node card • Provides four (4) Transmit and four (4) Receive pairs to test a complete AdvancedTCA channel • Edge-launch SMAs for superior bandwidth and ease of test cable attachment • Differential impedance of 100 W ±5% • SMT pads provided on Receive channels • Cut-outs for cable access to receive pairs and ease of card insertion/removal • Rx channels capable of utilizing high bandwidth coaxial blocking capacitors • Eliminate dependency on logic card availability for system evaluation • Verify and evaluate design compliance with AdvancedTCA guidelines

ROUTERS/SWITCHES

DSS Networks

Website: www.dssnetworks.com
Model: Model 5468 Switch **RSC No:** 20480
Fourth-generation BCM5388 Layer-2 switch; Intel 82546 dual-port PCI-X MAC host interface • 133/100/66-MHz, 32/64-bit PCI-X bus interface; PMC-Sierra PM8363 quad gigabit SERDES transceiver • Onboard FPGA for management, control, and routing functions; high-performance wire speed on all ports, 16 Gb total • Up to 16 M frames per second maximum switching rate; onboard firmware for configuration, management, and monitoring • 1.5 Mb of onboard memory for packet buffering; Extended Ethernet frame sizes to 9 KB; fully IEEE 802.3-compliant • PCI Rev. 2.2 and PCI-X 1.0-compliant; VxWorks 5.5 and Linux 2.4.xx driver support; FCC certified (pending)

SCSI PERIPHERAL

Red Rock Technologies

Website: www.RedRockTech.com
Model: RRTC-1SFA-LW **RSC No:** 20468
Capacity of up to 96 GB; no additional software is required for operation as a SCSI bootable drive • CompactPCI form factor occupying one 6U slot • Ultra Wide SCSI LVD interface available at front panel and J5 connectors • Can be configured for 8-bit, single-ended, and/or SCSI-2 operation, thus supporting legacy systems • Front panel status and activity LEDs • Rear Transition Module available

SHELF & MECHANICAL COMPONENTS

Schroff

Website: www.schroff.us
Model: AdvancedTCA Systems **RSC No:** 20417
2 to 16-slot AdvancedTCA systems ideal for telecom and networking applications • Broad range of configuration options available • Backplanes available in a variety of topologies including full mesh, dual star, and dual-dual star • Backplanes meet high-speed requirements of next-generation boards • Low cost, field replaceable fan trays reduce labor and maintenance costs • Removable fan trays provide exceptional cooling up to 200 watts

SOFTWARE: DEVELOPMENT TOOL

Performance Technologies

Website: www.pt.com
Model: NexusWare Core **RSC No:** 20813
A full Linux-based operating system • Linux ker-

nel is specifically tailored toward embedded applications • Complete suite of development tools and compilers, including the Eclipse platform • Powerful APIs for all onboard hardware resources • Integrated drivers: no need for external bus drivers • Application development with Windows XP/2000, Linux, or Solaris OS • Pre-packaged applications and protocols

SYSTEM MANAGEMENT

Adax

Website: www.adax.com
Model: Adax Signaling Products **RSC No:** 20553
Building blocks for system developers; signaling communications controllers and lower layer protocol software • Integrated software and blades for application developers; integrated signaling protocol stacks • Complete signaling gateways for everyone; multipurpose signaling gateways • Signaling nodes – SS7 or IP based STPs, HLR, VLR, SMSCs, databases, and more • Signaling gateways and IP signaling points for SS7 and IP switching, routing, back-haul, and tunneling • Media gateways, media gateway controllers, and softswitches • GPRS and 3G nodes including SGSNs, GGSNs, MSCs, RNCs, and Node Bs • Simulation, monitoring, and billing systems for test and measurement applications • Narrowband signaling for PSTN, GSM, and GPRS networks – SS7 (64k and 2 Mbs HSL), Frame Relay, LAPB/D/V5, and X.25 • Broadband signaling for 3G networks – ATM AAL2 and AAL5, SSCOP/SSCF, SSSAR/SSTED, IP over ATM, and Frame Relay • SIGTRAN signaling for fixed and mobile networks – SCTP, M2PA, M2UA, M3UA, and SUA with SIP interworking • SS7/IP interworking providing the ability to interconnect all three via T1/E1, OC3/STM-1, and Gigabit Ethernet

TELECOM

SBS Technologies

Website: www.sbs.com
Model: TELUM 1000 **RSC No:** 20429
155 Mbps full duplex line speed • PCI Express interface; PCIe Rev 1.0 compliant; support for a full-duplex OC-3 Interface • Support for 16,000 VCCs; 4 MB local memory • Optional Automatic Protection Switching (APS) • Passes and manages AAL1, AAL2, and raw cells • Segmentation and reassembly of AAL0, AAL3/4, and AAL5 cells • Traffic management supported: ABR, CBR, UBR, and VBR • Single or APS port versions • Supports ATM Forum UNI 3.1 and TM 4.0 • Intelligent Platform Management interface; onboard microcontroller-based subsystem • Hot-swap compliant • Support available for Linux, VxWorks, and Windows 2000/XP

Transtector Systems

Website: www.transtector.com
Model: ALPU Series **RSC No:** 21158
Auxiliary Lightning Protection Unit • Suitable for protecting Gigabit Ethernet systems using fast-acting silicon avalanche suppression diodes and reduced capacitance protection circuitry that permits high signal bandwidth • More than 12 different configurations are available on 2 week lead times • Clamping performance of SASDs while maintaining a TIA Cat-5e compliant network connection • Deliver protection to IEC 61000-4-5 standards • Can protect up to eight Cat-5e pairs as well as several configurations of DC power for POE applications • Designed to self-sacrifice in the event of a catastrophic event, taking protected equipment offline • 5.5 inches high, by 4 inches wide and 3 inches deep • Metal or plastic enclosures are rated NEMA 3R rainproof

TELEPHONY: VOIP

NMS Communications

Website: www.nmscommunications.com
Model: MG 7000A **RSC No:** 20393
480 IVR, fax, conferencing, VoIP, 3G 324M video sessions • 16 T1/E1 ports • Call control for CAS, ISDN, and SIP

THERMAL MANAGEMENT

Radian Heatsink

Website: www.radianheatsinks.com
Model: ATCA BGA Heatsinks **RSC No:** 20383
Removable ATCA BGA heatsinks can be installed with no special board modifications needed • Standard BGA heatsink sizes range from 21 mm to 45 mm footprints • Heatsink heights available from 7.11 mm to 9.8 mm for low-profile CompactPCI, AdvancedTCA, and PC/104 applications • Attachment options compatible with various chip heights and package types, including plastic, ceramic, and metal • Black anodized plating delivers enhanced performance in harsh environments and natural convection • All products provided pre-assembled, with lightweight aluminum heatsink, selected clip size, and thermal pad option

TURNKEY SYSTEM

Motorola

Website: www.motorola.com/computers
Model: Centellis CO **RSC No:** 20521
Centellis CO 21KX features: 12U/19" CompactPCI framework to deliver 5-nines availability • Fault-resilient design minimizes hardware induced failures • CompactPCI hot swap capability minimizes mean-time-to-repair • PICMG 2.16-compliant packet switching backplane • Ethernet switches and shelf controllers on same board, redundant and hot-swappable • Designed for NEBS Level 3 for telecom Central Office (CO) applications • EndurX CO 21KX features: PICMG 2.16-compliant CompactPCI packet switching backplane with 19 6U node slots • Dual redundant Carrier Grade Linux/Intel architecture processor-based nodes • Redundant Layer 2 Gigabit Ethernet switches and shelf management controllers • High availability framework API for HA-aware applications • Policy-driven event handling/propagation • Flexible software upgradability

Pinnacle Data Systems

Website: www.pinnacle.com
Model: TS2100 Telco System **RSC No:** 20413
2.0 GHz, low voltage, Xeon processor • One- or two-way configuration • L2 cache with integrated 512 KB • Memory: four DIMM sockets for up to 4 GB DDR266, registered • SDRAM, 72-bit, ECC, 184-pin 256 MB, 512 MB, 1 GB, 2 GB • Front Panel I/O: One USB 2.0 port • One serial RJ-45 port • Fibre: Two small form-factor pluggable connections • LEDs for status, health, hard drive activity, and Ethernet/FibreChannel connections • Switch Connections: Backplane 12 x 10/100/1000 Mbps Ethernet, Front Egress: 3 x 10/100/1000 Mbps Ethernet • InterSwitch Link: 1 x 10/100/1000 Mbps Ethernet • Chassis: 13U – 22.75" (577.85 mm) by 18.00" (508 mm) (D) by 19.00" (482.60 mm) (W) • Four fans cable mgmt filter • System power: One power distribution board • Support for up to four –48V DC Power Entry Modules (PEMs) • Backplane: 14-slot full mesh,12 system slots, two switch slots

SBS Technologies

Website: www.sbs.com
Model: AVC-cPCI-3003-3U **RSC No:** 20512
Lightweight – less than 11 pounds (4.9 kg) including modules • Compact for use in small spaces • Six, 3U CompactPCI slots • CM4 single board computer with 750/755 400-500 MHz processor, two 1 MB L2 cache, 1.6 GB/s • MIL-C-38999 Series III connectors • COTS AVC rugged conduction cooled chassis

Sun Microsystems

Website: www.sun.com
Model: Netra CP 2300 **RSC No:** 20504
Part of a comprehensive line of NEBS certified systems, storage, and management/availability software from Sun • Solaris OS operating environment • 650 MHz UltraSPARC IIi processor • Up to 2.5 GB memory (512 MB minimum) • A rack-mount architecture, CompactPCI compliant, and adherence to PICMG standards

RSC 20504

VIDEO: FRAME GRABBER

SBS Technologies

Website: www.sbs.com
Model: AVC-cPCI-3009 **RSC No:** 20562
COTS rugged conduction cooled chassis • 6 3U CompactPCI slots • MIL-C-38999 connectors • 9.5 pounds with modules • 5.0" (H) x 8.73" (W) x 8.75" (D) • Power supply: 100 watts, single or dual • CR3 Single Board Computers: Intel Celeron processor, system controller, or peripheral card operation • MIL-STD-1553 interfaces: Two dual redundant channels, independent operation as a bus controller, remote terminal, and dual function bus monitor

WIRELESS: SDR

Innovative Integration

Website: www.innovative-dsp.com
Model: Quixote **RSC No:** 20448
600-MHz TMS320C6416 DSP; 2-6 MGate Virtex-II FPGA • 32 Mbytes SDRAM, 8 Mbytes ZBT SBSRAM; 64/32-bit CompactPCI, 66 MHz, 5 V/3.3 V • AD6645 and AD9764 converters • Complex triggering modes with HW event logging • PMC site w/Jn4 to FPGA DIO • PICMG 2.17 StarFabric-compliant

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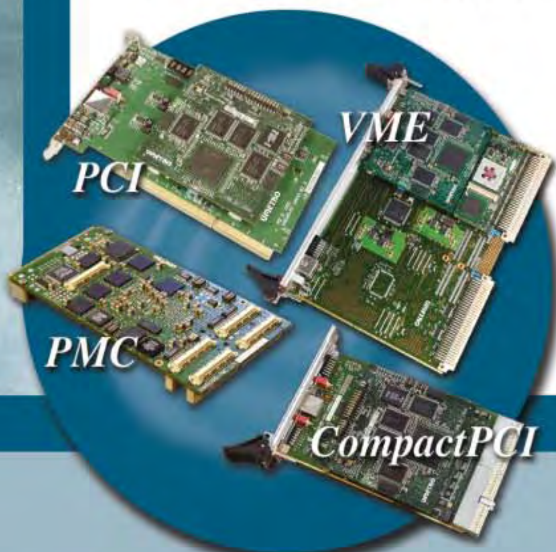

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